DESIGN OF AN INTRA-BUNCH-TRAIN FEEDBACK SYSTEM FOR THE EUROPEAN X-RAY FEL

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Abstract

After joining the preparatory phase of the European X-ray FEL project, the Paul Scherrer Institute agreed in taking over responsibility for electron beam stabilization by developing a fast intra-bunch-train feedback (IBFB) system, which will be tested in its prototype version at the FLASH linac of the collaboration partner DESY. The proposed IBFB topology consists of two beam position monitors ("upstream BPMs") followed by two kicker magnets for each transverse plane and two more BPMs ("downstream BPMs"). By measuring the position of each bunch at the upstream BPMs and applying suitable transverse kicks individually to the following bunches, the architecture of the FPGA-based digital IBFB electronics (with a latency preferably below the bunch spacing of 200 ns and 1000 ns for the XFEL and FLASH) allows to damp beam motions up to hundreds of kHz. In addition to the FPGA-based feedback, DSPs enable adaptive feed-forward correction of repetitive beam motions as well as feedback parameter optimization using the downstream BPMs. This paper gives an overview of the architecture and status of the IBFB subsystems being developed, like stripline BPMs, digital electronics, and kicker magnets.

INTRODUCTION

In order to guarantee the stable SASE operation of the European X-ray FEL (XFEL) at its 1 Å target wavelength, the 1 nC 20 GeV electron beam of the XFEL main linac requires a transverse RMS position stability in the order of 10% of the ~30 µm beam size σ in the undulators [1]. In contrast to other proposed linac-based FELs that use single bunches with repetition rates in the order of 100 Hz, the XFEL will have bunch trains of up to 3250 bunches and 200 ns bunch spacing at 10 Hz repetition rate.

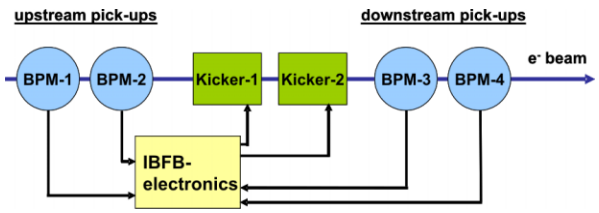

Figure 1: Proposed IBFB Topology.

When installed behind the main linac, the measurement and correction the of transverse position in both planes on a bunch-by-bunch basis would allow the proposed IBFB system [2] to damp harmful beam position perturbations up to frequencies of some 100 kHz that may originate from noise sources like cooling water and helium flow, ground motions, power supply jitter, switching magnets, RF transients and jitter, photo-cathode laser jitter and related beam current variations as well as long range wakefields. Table 1 contains a summary of the IBFB specifications for the prototype system to be tested at FLASH as well as for the final system for the XFEL. The following sections give summaries of the design and status of the different IBFB subsystems.

Table 1: Transverse IBFB Specifications

Transv. IBFB Specifications	**FLASH**	**XFEL**
bunch-by-bunch stability - at location of IBFB - along undulators	< σ/10 5 - 15 µm < 5 µm	< σ/10 3 - 10 µm < 3 µm
max. beam position offset - at location of the pick-ups	< 10 · σ < 1.5 mm	< 10 · σ < 1 mm
bunch-by-bunch resolution	≤ 2 µm	≤ 1 µm
system latency	< 1000 ns	< 200 ns

RESONANT STRIPLINE BPM

The IBFB needs a BPM pickup that generates a signal which is short compared to the desired IBFB latency of about 200 ns, and that is also large enough to be safely above the electronics noise level limits for the desired resolution of 1-2 µm. Therefore a novel resonant stripline pickup was developed in a collaboration of PSI (concept [4] and electromagnetic design) and DESY (mechanical construction and UHV/dust-free compliant production). So far one pickup was installed at the DESY flash facility and three in the SLS booster that has a bunch charge and repetition rate similar to FLASH (up to 1 nC, 1 µs) but provides more space, which allowed to install three pickups in a single straight section for beam-based noise correlation measurements.

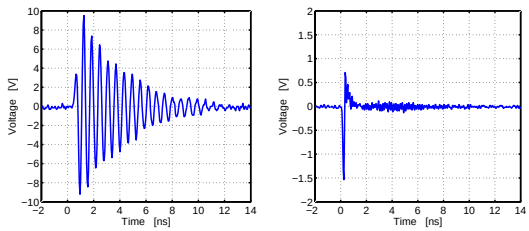

Figure 2: Comparison of beam induced signal at resonant stripline pick-up (left) and button pickup (right).

*Work supported by Swiss State Secretariat for Education and Research SER

Fig. 2 shows the low-pass filtered signal of a resonant stripline pickup at the SLS booster for ~0.5 nC bunch charge. Compared to typical button and non-resonant stripline pickups, the usable signal level and energy content is much larger, with only ~10 ns decay time.

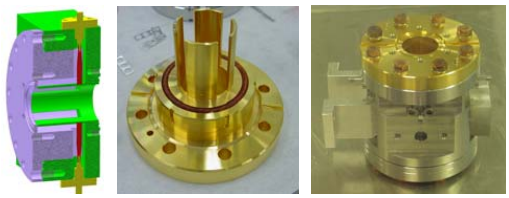

Figure 3: Resonant Stripline BPM Pickup.

Measurements with a BPM test bench consisting of 2D motorized stages and a 50 ohms matched inner conductor built at PSI as well as measurements performed at DESY allowed to identify and optimize critical points of the design. Following the original prototype, a refined version has been built, which will be used for the IBFB prototype system. The frequencies of monopole (1.615 GHz), dipole (1.653 GHz) and quadrupole (1.677 GHz) modes as well as internal and external Q factors obtained from measurements for the optimized design are in good agreement with theoretical predictions.

CAVITY BPM

In addition to the resonant stripline that will be used as "workhorse" BPM for first tests of the IBFB at FLASH, a cavity BPM was designed and built at PSI [2] in collaboration with a company in order to study the feasibility of ultra-high resolution BPMs for the final XFEL IBFB. The BPM consists of a 4.3896 GHz monopole cavity to be used as a beam current reference and a 4.3875 GHz dipole cavity where the TM11 mode couples to external waveguides where it is extracted using capacitively coupled SMA feedthroughs for position measurement while the TM01 mode coupling is suppressed. The dipole cavity was recently delivered to PSI and is ready for tests on the BPM test bench.

RF FRONT-END

Fig. 4 shows the proposed architecture of the RF front-end (RFFE) for the resonant stripline BPM for one transverse plane. The signals of opposite pickup electrodes are filtered, and a 180° hybrid separates the monopole mode signal (Σ) that is proportional to the beam current from the dipole mode signal (Δ) that is proportional to the beam position times the current. The resulting signals pass variable gain amplifiers and are then mixed down to DC using tunable PLLs that use a machine reference clock to synthesize the desired frequencies. The mixed signals are filtered, and the resulting pulses of about 15 ns length are available at the RFFE outputs for digitization. In order to achieve optimal separation of strong monopole and weak dipole mode (-75 dBc for 1 µm), amplitude and phase tuners in front of the hybrid will be periodically adjusted during the time in between two bunch trains using a sinusoidal pilot signal that is coupled into the complete signal chain. See Ref. [2] for further details. So far most parts of the modular RFFE design have been fabricated. At present different input filter designs for the RFFE are being characterized and compared to simulations, with signals of the three pickups recently installed in the SLS booster allowing to find an optimal compromise between monopole signal suppression, filter latency, insensitivity to component tolerances, and effort for calibration and tuning.

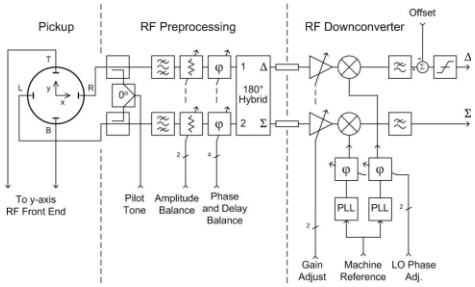

Figure 4: Proposed BPM RF front end (x-axis only).

DIGITAL ELECTRONICS AND CORRECTION ALGORITHM

Fig. 5 shows the architecture of the PSI DSP Carrier (PDC) board, a VME/VXS board that is being developed at PSI to serve as data processing back-end for the IBFB. The PDC is based on the PSI "VPC" board [3], but uses two high-performance TS201 "TigerSHARC" DSPs instead of one low-cost DSP, four Virtex-4 instead of two Virtex-2 Pro FPGAs, 100 times more RAM, multi-gigabit LVDS mezzanine connectors instead of PMC connectors, and the VXS standard for multi-gigabit communication between PDCs via the VME/VXS crate backplane. For the IBFB the PDC will be equipped with two mezzanine modules that are being developed. Each contains four 12-bit 500 Msps ADCs with 4.5 samples latency that are used to digitize the ~15ns long Σ and Δ pulses of two RFFEs, and two 14-bit DACs with max. 1 Gsps sample rate and 18 samples latency to drive the kicker magnet amplifiers.

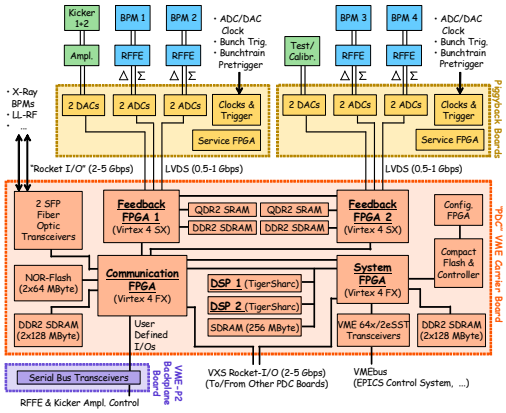

Figure 5: IBFB digital signal processing hardware architecture: PDC board with ADC/DAC mezzanines.

ADCs and DACs of each mezzanine are connected to Virtex-4 SX "Feedback" FPGAs on the PDC (one FPGA per mezzanine). These FPGAs calculate the beam positions and kick amplitudes using an FIR-based

feedback algorithm that predicts the kick necessary to correct the position of bunch no. N from the positions of bunches N-1, N-2, N-3 etc. Only the upstream BPM data is used to predict these kicks (using a beam optics model), since the maximum latency allowed for the electronics using the upstream BPMs is 200 ns minus the *difference* of cable delays and electron flight time from BPM1 to kicker 2 (see Fig. 1), while the latency budget when using the downstream BPMs would be 200 ns minus the *sum* of the cable delay BPM4-kicker1 and flight time kicker1-BPM4 (since the cable signal and electrons travel in opposite directions). However, the downstream BPM data will be used to check and automatically correct and optimize the model used for the calculation of the kicks.

In addition to a bunch-by-bunch feedback, the two TS201 DSPs on the PDC board will perform an adaptive feed-forward algorithm to correct beam motions that are the same from bunch train to bunch train. The DSPs will calculate lookup tables for beam positions to be subtracted and kicks to be added by the Feedback FPGA (see Fig. 6) for each bunch, so that the actual feedback algorithm just needs to correct non-repetitive beam motions that are different from bunch train to bunch train.

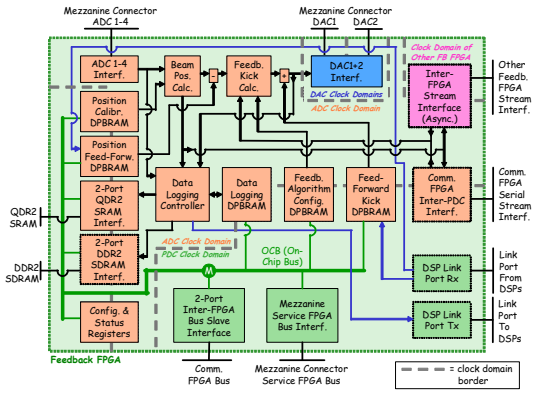

Figure 6: Firmware architecture of the Virtex4-SX "Feedback" FPGA on the PDC board.

The PDC board can be used in two possible configurations: a) one PDC handles all four RFFEs and two kickers for one plane, another PDC handles the other plane, or b) one PDC handles all RFFEs of the upstream BPMs and all kickers for both planes, and another PDC handles the downstream BPMs for both planes. Data exchange between two PDCs or between PDCs and other accelerator subsystems is possible using multi-gigabit links on the PDC front-panel (SFP) or on the VME/VXS backplane. Since these links have latencies in the order of 100-300 ns (depending on baud rate and protocol used), the above mentioned configuration a) will only be used if the coupling between both planes is so small that it does not have to be accounted for on a bunch-by-bunch basis (e.g. by rotating hor./vert. position vectors), since the position data cannot be transmitted from one PDC to the other fast enough (for the XFEL). Configuration b) allows to use the data of both planes of all upstream BPMs to calculate the kicks for each of the four kickers by using low-latency links between the two Feedback FPGAs on the same PDC, at the expense of longer latency for the downstream BPM data transfer via gigabit links.

The PDC schematics, mechanical design and PCB component placement is finished and the layout (~22 layers) is in progress. First prototype tests of PDC and mezzanine are scheduled for autumn 2007. Apart from the IBFB, the PDC could also be used e.g. for multibunch feedbacks or global orbit feedbacks in storage rings.

KICKER DESIGN

The beam position corrections for the IBFB will be applied by two kicker magnets for each plane. Fig. 7 shows a stripline kicker designed at PSI that will be built until end 2007 and installed for tests of the IBFB at FLASH in 2008. The stripline shape matches the beam pipe diameter of 34 mm. Fig. 8 a) shows the computed S parameters of the structure. The kicker bandwidth (green curve, x=50 MHz/div., y=10dB/div., scale=-70...0 dB) exceeds the desired value of 50 MHz. Reflections (red curve) are below -25 dB, which is excellent. In Fig. 8 b), we see the deflecting electrical field in the stripline center vs. frequency (x=100 MHz/div., y=200V/div., scale=0...800V). The resulting correction kick is expected to be 16 µrad at 1 GeV using 25 kW input power per port.

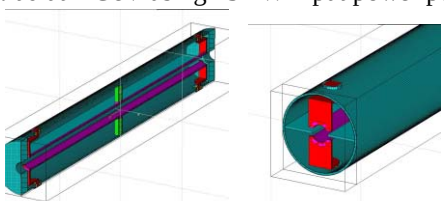

Figure 7: 3D views of vertical IBFB stripline kicker.

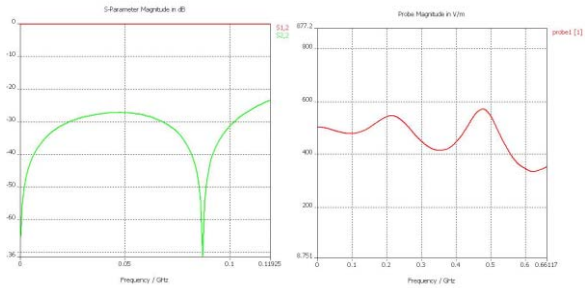

Figure 8: a) Simulated S-parameters (left side) and b) transverse electrical field strength of IBFB stripline kicker (right side).

REFERENCES

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