APPLICATION OF A 5 GSPS ANALOGUE RING SAMPLING CHIP FOR LOW-COST SINGLE-SHOT BPM SYSTEMS

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Abstract

In contrast to storage ring BPMs with continuously sampling ADCs, BPMs of single-bunch linear accelerators with typical repetition rates of 10-100Hz may also use waveform digitisers that sample just during a short interval when the bunch is passing the pickup. At PSI a 12-channel analogue sampling chip called "DRS" has been developed [1] that samples input signals in an array of 1024 capacitors per channel at up to 5GSPS. The acquisition can be stopped by a trigger signal and then the capacitor voltages of all 12 channels can be digitised with a single commercial external ADC at 33MSPS, achieving ~11 bit effective DC resolution and 450MHz max. bandwidth. The DRS chip was originally developed for low-cost digitization of 3000 detector signals of a particle physics experiment, using the PSI "VPC" VME64x FPGA board [2] as digital back-end equipped with two PMC mezzanine modules with two DRS chips each. However, such DRS-based systems are also an attractive solution for inexpensive direct sampling and FPGA-based post-processing of suitable BPM pickup signals. This paper discusses BPM-related properties, limitations, possible improvements and measurement results of DRS-based electronics.

INTRODUCTION

RF beam position monitor (BPM) electronics for narrowband pickup signals with typical frequencies from hundreds of MHz to many GHz traditionally required an RF front-end (RFFE) that usually contained mixers to convert the pickup signals down to frequencies that can be sampled by standard analogue-to-digital converters (ADCs). While progress in ADC technology has shifted the frequency limit where pickup signals can be sampled directly (without need for a mixer-based RFFE) to the GHz-range, suitable commercially available fast ADCs require quite some power and a significant amount of electronics infrastructure for clocking, triggering and high-speed readout.

In contrast, solutions based on the DRS chip require just a single comparatively slow ADC with few low-speed digital connections e.g. to a field programmable gate array (FPGA) in order to digitise up to 12 input signals per DRS chip with 1024 samples per signal at up to 5 GSPS, without need for an external clock, high-precision trigger, or large numbers of differential high-speed FPGA connections. In addition to the comparatively low costs and low power of only 10mW per DRS chip channel this makes DRS-based electronics a potential candidate e.g. for BPMs in the injector or transfer lines of linac-driven single-bunch FELs like the planned PSI FEL [3] where typical resolution requirements in the order of 10-20μm are relaxed compared to the BPMs in the FEL undulator sections where stable lasing and related beam-based trajectory and magnet alignment may require a resolution and drift in the micron or even submicron range.

Pickup Types

While undulator BPMs of linac-based FELs often use cavity pickups with multi-GHz signals and mixer-based electronics for highest resolution, the remaining part of the linac may also use less sophisticated BPM systems with capacitive button or so-called resonant stripline pickups [4]. While the frequencies of common cavity pickups are far above the DRS chip bandwidth, resonant striplines or button pickups with lowpass or bandpass filters at frequencies of 500MHz or less are possible candidates for DRS-based direct sampling. Resonant stripline BPM pickups were pioneered at PSI by M. Dehler and are used e.g. in the SLS linac and transfer lines. They consist of four in-vacuum λ/4 strip resonators parallel to the beam, having 90° rotation symmetry with respect to the beam axis. Their decaying sinusoidal signals are extracted by one orthogonal vacuum feed-through antenna per strip. The loaded Q depends on the distance of the antenna tap point to the shorted end of the strip. The frequencies of the fundamental monopole, dipole and quadrupole modes depend mainly on the strip length. Mode frequency differences of typ. < 3% cause negligible frequency "beating" for sufficiently low Q values. The remainder of this paper discusses the architecture as well as lab and beam measurements of DRS-based prototype electronics built at PSI to evaluate the usability of the DRS chip for BPM systems.

HARDWARE

The DRS Chip

The developed prototype electronics uses version 3 of the DRS chip ("DRS3") [5]. The sampling process is started by an external pulse whose leading edge propagates through a "domino" ring of inverters on the chip (see Fig. 1), with two inverters per sampling cell. A "tail-biting" circuit ensures that each element of the inverter ring is reset to its initial state shortly after the leading edge has passed the inverters of a cell, which results in a pulse ("domino wave") that circulates periodically through the inverter ring. During the short duration while the pulse passes a sampling cell, two "write" switches are closed that connect the two electrodes of the ~220fF sample/hold capacitor of that cell to the differential input pins of the respective channel. Since all capacitors of all 12 channels are controlled by the same domino wave, all channels have the same sampling rate that can be adjusted between 10MSPS and 5GSPS by an external voltage which determines the

propagation speed of the domino wave. In addition to a continuous sampling mode where the wave is circulating until stopped by an external trigger, the DRS3 chip also supports a "single shot" mode where the wave is started by a trigger and stops after one revolution.

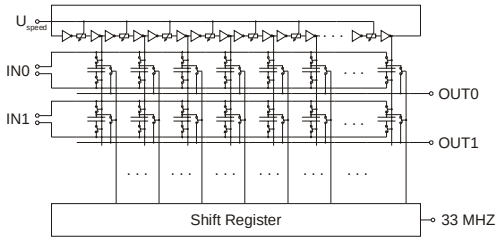

Figure 1: Simplified Schematic Operating Principle of the DRS Chip.

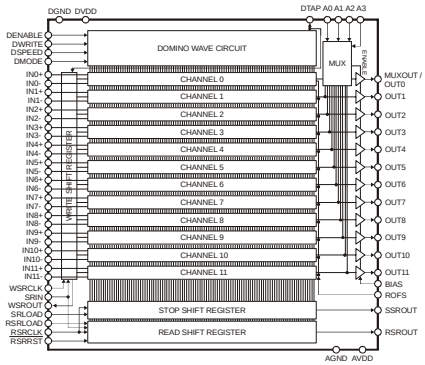

Figure 2: DRS3 Chip I/O Connectors and Architecture

DRS PMC Mezzanine and VPC Board

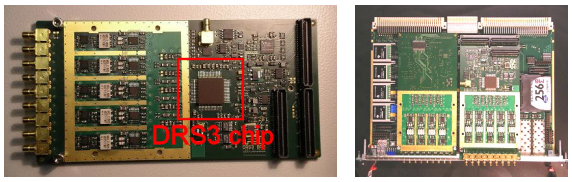

Figure 3a: 9-Channel DRS-based digitiser PMC mezzanine module for the PSI VPC board. Figure 3b: PSI VPC VMEbus board with one DRS mezzanine plugged (left) and one unplugged and flipped (right).

Fig. 3a shows a PMC mezzanine board that was designed at PSI. Its 9 single-ended SMB input connectors are AC-coupled to the differential inputs of a DRS3 chip via variable gain amplifiers with >40dB range that provide flexible level adjustment and optimal ADC resolution for various signal sources. A single 16-bit ADC on the PMC is used to digitize all DRS channels. Multi-channel DACs on the PMC are used to adjust the sample rate and to shift the DC-levels of the differential input pins and the readout pin of the DRS chip. This allows to maximise the ADC range both for unipolar and bipolar input signals. The DACs were also used for in-situ DC calibration and linearity correction of each sampling capacitor of the DRS chip using 10-point lookup tables. Electronic input switches allow to connect a common AC calibration signal instead of the SMB inputs to all DRS chip inputs. Two PMCs can be plugged onto the PSI "VPC" VMEbus board (Fig. 3b) where a Xilinx Virtex2-Pro FPGA controls the ADC, DACs, switches etc. via user-defined I/Os and allows to read the sampled data via VMEbus. One of the 9 SMB inputs also serves as trigger to start the sampling in single-shot mode.

MEASUREMENT RESULTS

Temporal Nonlinearity and Random Jitter

Due to systematic and random manufacturing tolerances, the propagation speed of the domino wave varies from cell to cell, which causes signals to be sampled e.g. not exactly every 200ps but at non-equidistant time intervals. However, this "temporal nonlinearity" (called "fixed pattern jitter" in the DRS datasheet) is mainly systematic and reproducible.

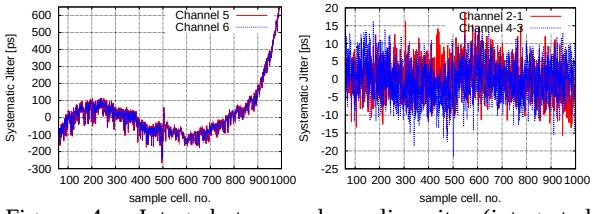

Figure 4a: Integral temporal nonlinearity (integrated "fixed pattern jitter") of the DRS chip at 5GSPS. Figure 4b: Difference of the integral temporal nonlinearity of two different channels.

Fig. 4a shows the measured integrated temporal nonlinearity of the DRS3 PMC obtained by a fit for 500 measurements per channel at 5GSPS with a 500MHz sine wave input signal. The amplitude, frequency and initial phase of a sine function were fitted individually for each measurement and channel. The time of the sampling points was fitted commonly for all measurements of each channel using only samples adjacent to zero-crossings of the signal in order to obtain the average fixed pattern jitter. The derivative of the curve in Fig. 4a (called "fixed pattern jitter" or differential temporal nonlinearity) is the temporal distance of adjacent samples minus the nominal (average) distance of ~200ps. The typical RMS fixed pattern jitter of a channel is ~46ps RMS at 5GSPS. The positive derivative between cell 0 and 200 in Fig. 4a means that the domino wave propagates below its average speed in this region. Between cell 200 and 600 it is running faster, after cell 600 slower again. Fig. 4b shows that the temporal nonlinearity is nearly identical for different channels, which is to be expected since the capacitors switches of all channels are driven by the same domino chain. This makes the DRS chip well suited for applications where the amplitude ratio of phase-matched input signals like the BPM pickup signals in Fig. 6a/b has to be measured and where the systematic variations and exact value of the sampling rate are of minor relevance. Fig. 5 shows the temporal RMS deviation of the measured data samples from the above mentioned fitted curves. The plot assumes that the deviation of the fitted curve from

the measured values originates only from random sampling jitter, neglecting amplitude noise. Therefore Fig. 5 gives an upper limit for the RMS random sampling jitter of the chip. The plot only shows the jitter for a fixed average revolution speed of the domino wave since the revolution frequency was one of the fit parameters. However, this is of minor relevance for practical BPM applications. If required, the revolution frequency can be measured either by an external pin of the DRS chip that toggles at each revolution or by sampling a reference clock signal on an unused channel.

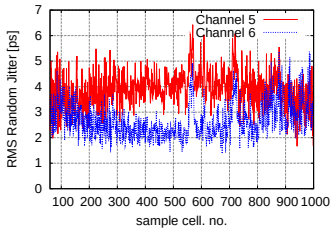

Figure 5: DRS3 random sampling jitter, best (2.7ps RMS) and worst (3.9ps RMS) channel of one chip.

Resonant Stripline Beam Tests

Fig. 6a shows the signal generated by a 0.4nC electron bunch of the SLS linac in a resonant stripline pickup that has ~500 MHz fundamental mode frequency. Fig. 6b shows the signal of opposite striplines, filtered with an additional 500MHz bandpass of ~10MHz bandwidth.

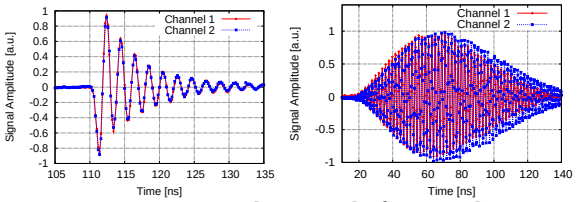

Figure 6a: Resonant stripline signal of an SLS linac BPM sampled with the DRS PMC at 5GSPS. Figure 6b: signals sampled using additional 500 MHz bandpass filters.

The SLS resonant stripline pickups for 40mm beam pipe diameter have diagonally arranged strips. The vertical beam position is $y = k\bullet((A+B)-(C+D))/(A+B+C+D)$, with k = 8.33mm. A, B, C and D are the signal amplitudes of the top left/right and bottom right/left strips. In order to estimate the achievable position resolution, the DRS PMC was fed with the beam signal of a single strip of an SLS linac BPM split onto four PMC inputs in order to pretend a perfectly centered electron beam. Fig. 7 shows the obtained RMS position resolution of 28.2µm for direct sampling of the strip signals and 8.6µm when using additional bandpass filters. It should be emphasised that the obtainable resolution also depends on the algorithm used to calculate the signal amplitudes from the sampled waveform. The positions plotted in Fig. 7 were calculated by applying the above mentioned formula only to the samples of a few large, most jitter- and noise-insensitive local maxima and minima of the sampled waveforms and by averaging these values for each bunch. More advanced fit-based algorithms are presently being evaluated. They may allow significantly improved position resolution by using more samples, by tolerating input signals that are not phase-matched, and by accounting for the known fixed-pattern jitter and bandwidth variations of the sampling cells.

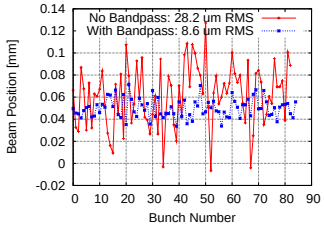

Figure 7: Single-bunch beam position, calculated from sampled SLS linac stripline signals with and without 500MHz bandpass filter.

SUMMARY AND OUTLOOK

The obtained test results indicate that DRS-based BPM electronics provide sufficient resolution e.g. for common transfer line BPMs. Other system characteristics like linearity and temperature drift as well as options for their in-situ measurement and FPGA-based periodic self-calibration are presently being investigated. The next chip version "DRS4" is expected to be available at PSI in a 10k quantity until fall 2008, with higher bandwidth, on-chip PLL, smaller chip size with improved grounding, and smaller AC bandwidth variations of the sampling cells. Further resolution improvements e.g. for stripline BPMs are possible by using the DRS4, by advanced amplitude fit algorithms, or by using analogue rather than digital signal subtraction techniques. Moreover, each BPM signal could be sampled by many DRS channels or chips in parallel in order to reduce statistical measurement errors. With power requirements of 120mW and costs of $15 per 8-channel DRS4 chip for 10k chip quantities and the possibility to use a common digitiser ADC for several DRS chips, such interleaved oversampling techniques may allow effective sample rates > 100 GSPS and even sub-micron BPM resolution at acceptable system costs, system power and PCB size requirements.

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[3] R. Bakker et al., "Status of the 250 MeV Test Injector for the PSI XFEL", this conference.

[4] M. Dehler, "Resonant Stripline BPM for Ultra Low Current Measurement", Proc. DIPAC´05, Lyon, France, June 2005, p. 284

[5] https://midas.psi.ch/drs/DRS3_rev1.pdf