APPLICATION OF A 5 GSOPS ANALOGUE RING SAMPLING CHIP FOR LOW-COST SINGLE-SHOT BPM SYSTEMS

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ABSTRACT
In contrast to storage ring BPMs with continuously sampling ADCs, BPMs of single-bunch linear accelerators with typical repetition rates of 10-100 kHz may also use waveform digitisers that sample just during a short interval when the bunch is passing the pickup. At PSI a 12-channel analogue sampling chip called "DRS" has been developed that samples input signals in an array of 5024 capacitors per channel up to 5 GSOPS. The acquisition can be stopped by a trigger signal and then the capacitor voltages of all 12 channels can be digitised with a single commercial external ADC at 33 MSOPS, achieving ~11 bit effective DC resolution and 450 MHz max. bandwidth.

The DRS chip was originally developed for low-cost digitization of 3000 detector signals of a particle physics experiment, using the PSI "VPC" VME64x FPGA board as digital back-end equipped with two PMC mezzanine modules with two DRS chips each. However, such DRS-based systems are also an attractive solution for inexpensive direct sampling and FPGA-based post-processing of suitable BPM pickup signals. This paper discusses BPM-related properties, limitations, possible improvements and measurement results of DRS-based electronics.

RESONANT STRIPLINE PICKUP
- PSI Design (M. Dehler)
- Four A4 resonators (1 beam)
- Antennas near shorted end
- Low-Q decaying sine signals
- Installed in SLS transfer lines & linac, 500 MHz
- L_strip=150 mm, 40 mm pipe
- Used for DRS BPM electronics test

Lab Test Results
- Integral Temporal Nonlinearity (ITN)
- Definition: Integral of deviation from nominal (average) sample period, e.g. 200 ps @ 5 GSOPS
- Systematic & random chip production tolerances: sample intervals not equidistant
- Predictable & reproducible ("fixed pattern jitter")
- Plot obtained via fit to 500 measurement sets

ITN Difference of Channel Pairs
- Sample period for each cell number nearly identical for all channels
- Reason: sample/hold switches of all channels switched by the same domino wave pulse
- Makes DRS chip well suited for measuring e.g. amplitude ratio of phase-synchronous BPM signals

Random Jitter
- Plot shows RMS deviation of measurement data from fitted average ITN, neglecting amplitude noise
- Domino wave revolution frequency jitter normalized out during fit, but revolution frequency can be measured via pin or by sampling a reference clock on an unused channel
- Channel dependent: best channel 2.7 ps RMS, worst channel 3.9 ps RMS

DRS CHIP/PMC MEASUREMENTS
- Resonant Stripline BPM Pickup Signals
  - Plot shows sampled 5 GSOPS DRS waveform for 500 MHz SLS linac resonant stripline BPM pickup
  - 0.4 nC beam charge
  - Amplitudes for beam position calculation determined from samples by software algorithm
  - Low Q -> few samples -> limited resolution

Bandpass-Filtered Res. Strp. Signals
- Plot shows resonant stripline signals filtered by additional external 500 MHz + 10 MHz bandpass
- Larger number of samples -> better resolution

Beam Position Resolution
- Beam position calculated from strip amplitudes: $P_{os} = 8.3\,\mu m \times (A+B-C)/(A+B+C)$
- Centered beam simulated by splitting signal of 1 strip to 4 inputs of DRS PMC
- Primitive algorithm to determine amplitude - use only few local minima/maxima of waveform: 28.2 $\mu m$ RMS position resolution without filter 8.2 $\mu m$ RMS with bandpass
- Evaluation of more advanced algorithms (fft, ...)
- To obtain amplitude using all samples, accounting for measured ITN & nonlinearity -> better resolution

SUMMARY AND OUTLOOK
The obtained test results indicate that DRS-based BPM electronics provide sufficient resolution e.g. for common transfer line BPMs. Other system characteristics like linearity and temperature drift as well as options for their in-situ measurement and FPGA-based periodic self-calibration are presently being investigated. The next chip version "DRS4" is expected to be available at PSI in a 10k quantity until fall 2008, with higher bandwidth, on-chip PLL, smaller chip size with improved grounding, and smaller AC bandwidth variations of the sampling cells. Further resolution improvements e.g. for stripline BPMs are possible by using the DRS4, by advanced amplitude fit algorithms, or by using analogue rather than digital signal subtraction techniques. Moreover, each BPM signal could be sampled by many DRS channels or chips in parallel in order to reduce statistical measurement errors. With power requirements of 120 mW and costs of 15 $ per 8-channel DRS4 chip for 10k chip quantities and the possibility to use a common digitiser ADC for several DRS chips, such interlaced oversampling techniques may allow effective sample rates > 100 GSOPS and even sub-micron BPM resolution at acceptable system costs, system power and PCB size requirements.