The "Generic VME PMC Carrier Board"

Status and Perspectives of a Common Digital Platform for Beam Diagnostics and Feedbacks at PSI

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Motivation

- PSI diagnostics section: several new projects (e-,p+,γ,μ)
  - New proton DBPM
  - Integration of photon BPMs into SLS-FOFB
  - Cooperation: μ-decay detector readout (~3000 chan., 2-4 GSa/s, 1024 samples/chan.)
  - PROSCAN, LEG, Femto, DESY-RF cooperation, ...
- Need monitor electronics: analog & (growing) digital part (filter, analysis, feedback link, ...) that dominates complexity/man power (HW,FW,SW), e.g. SLS DBPM1

→ Customized analog/digital front-ends
→ Common digital back-end HW for all monitors
→ (Some) common firmware/software

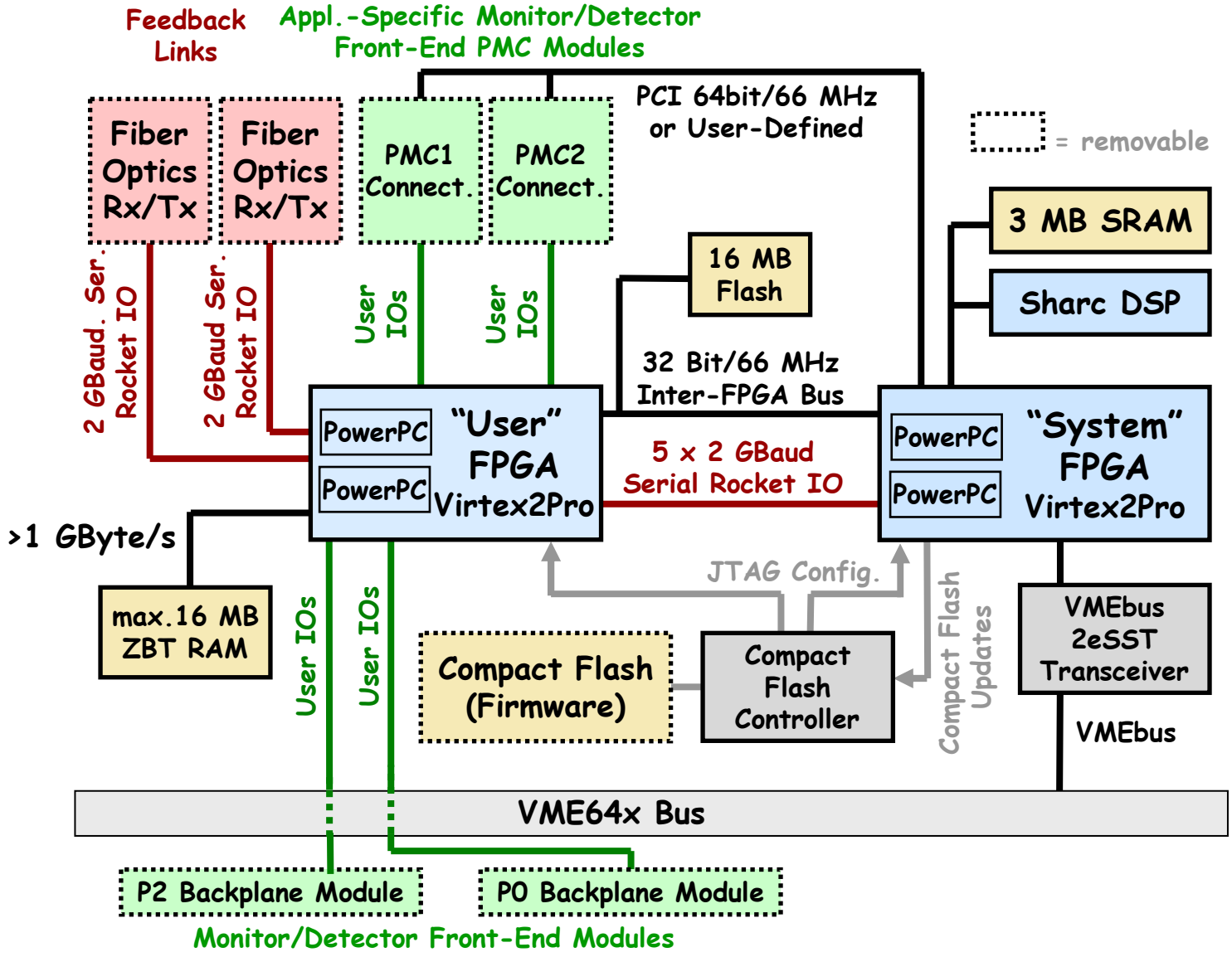
Strategy (Back-End Hardware)

- Reconfigurable → FPGAs
- Minimum number of ICs
- Shift complexity from HW(ASICs) to FPGA FW(VHDL)
- High-level algorithms in the monitor → µP and/or DSP
- Feedback-ready → multi-gigabit fiberlink
- „System-On-A-Chip" (µPs, RAM, Clk, MGB-SerDes, ...)
- VME64x (PSI standard)

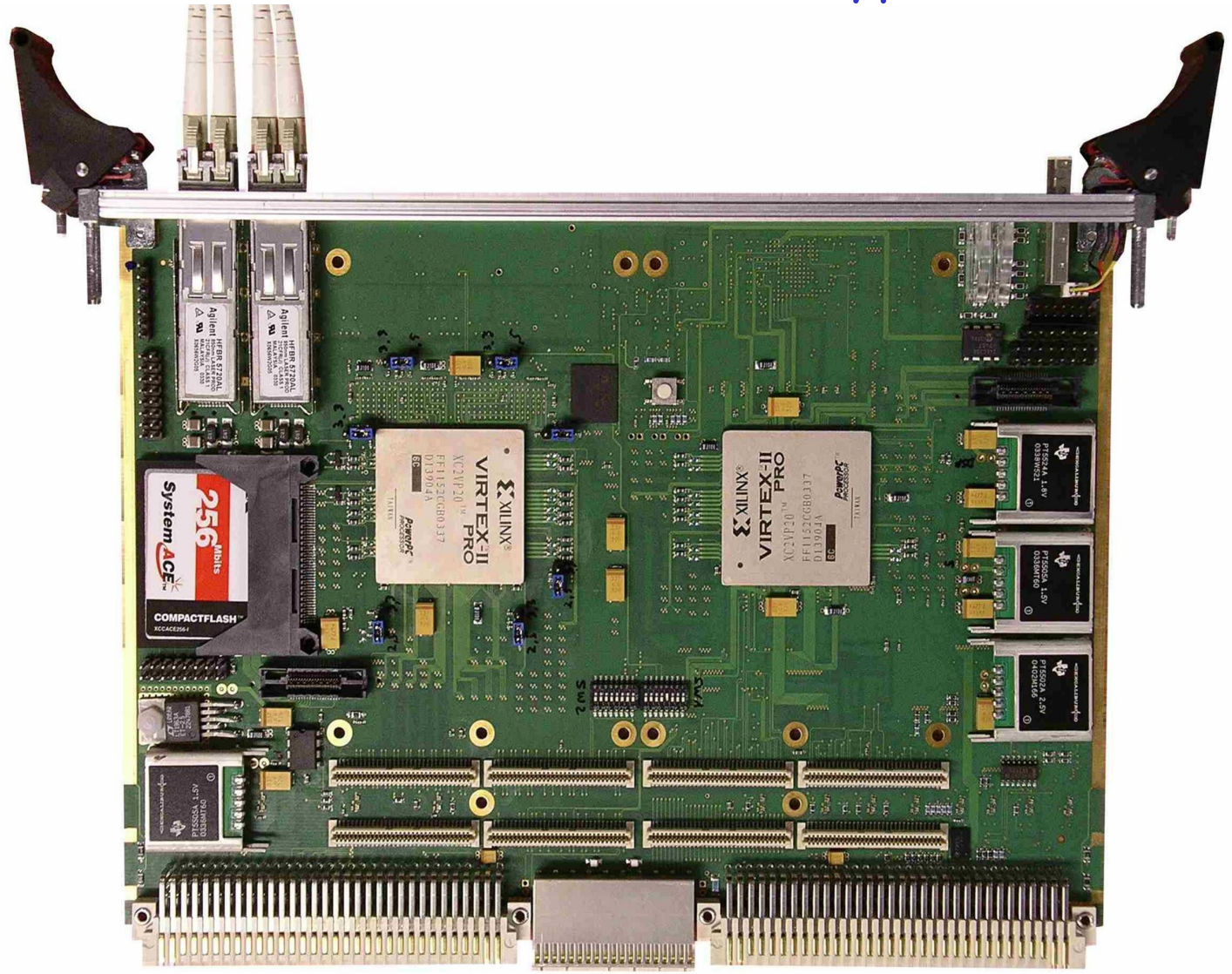
Strategy (Firmware/Software)

- Portable → VHDL, C
- Many common ("generic") & few application-specific modules

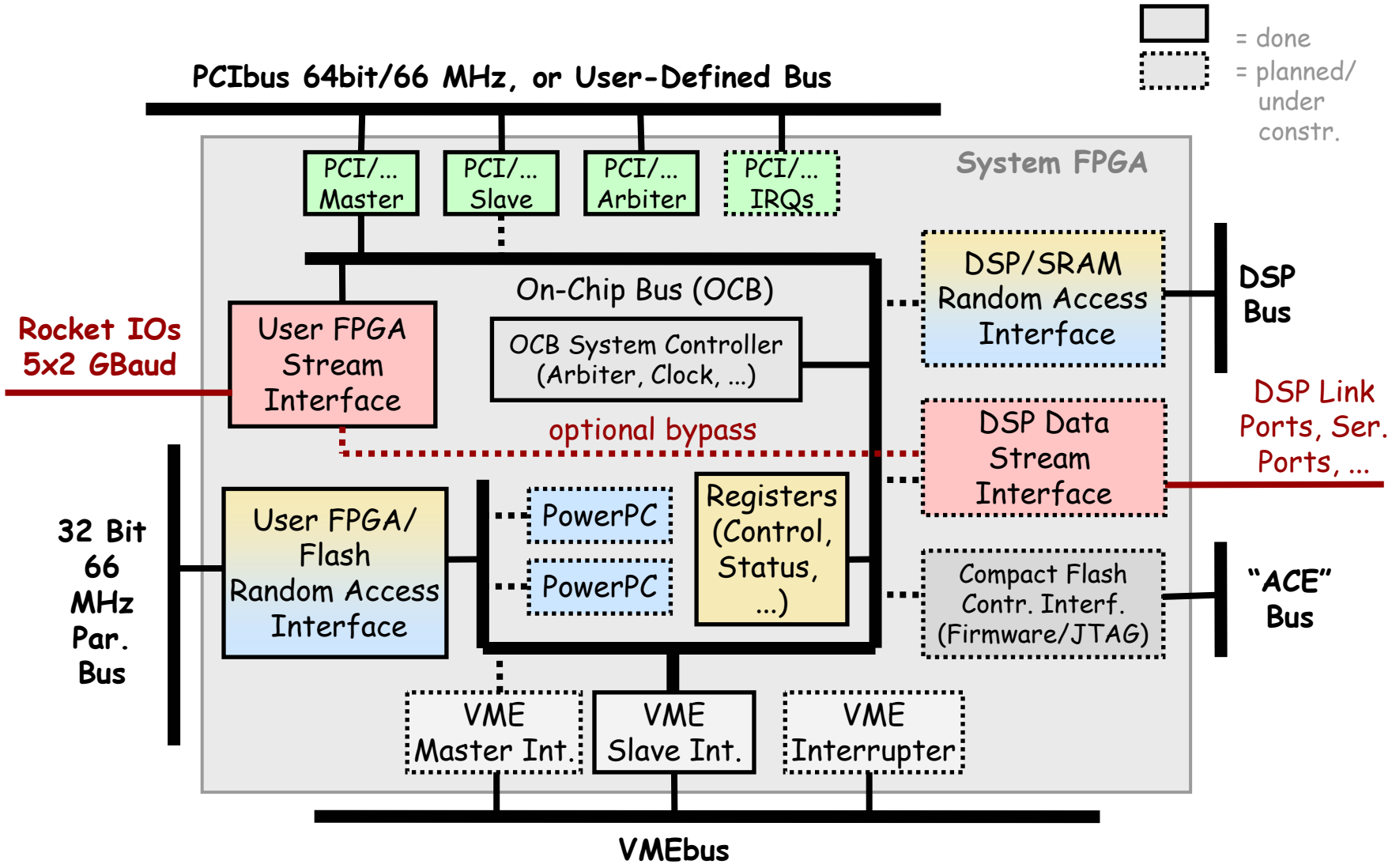
"VPC" Board: Hardware Architecture



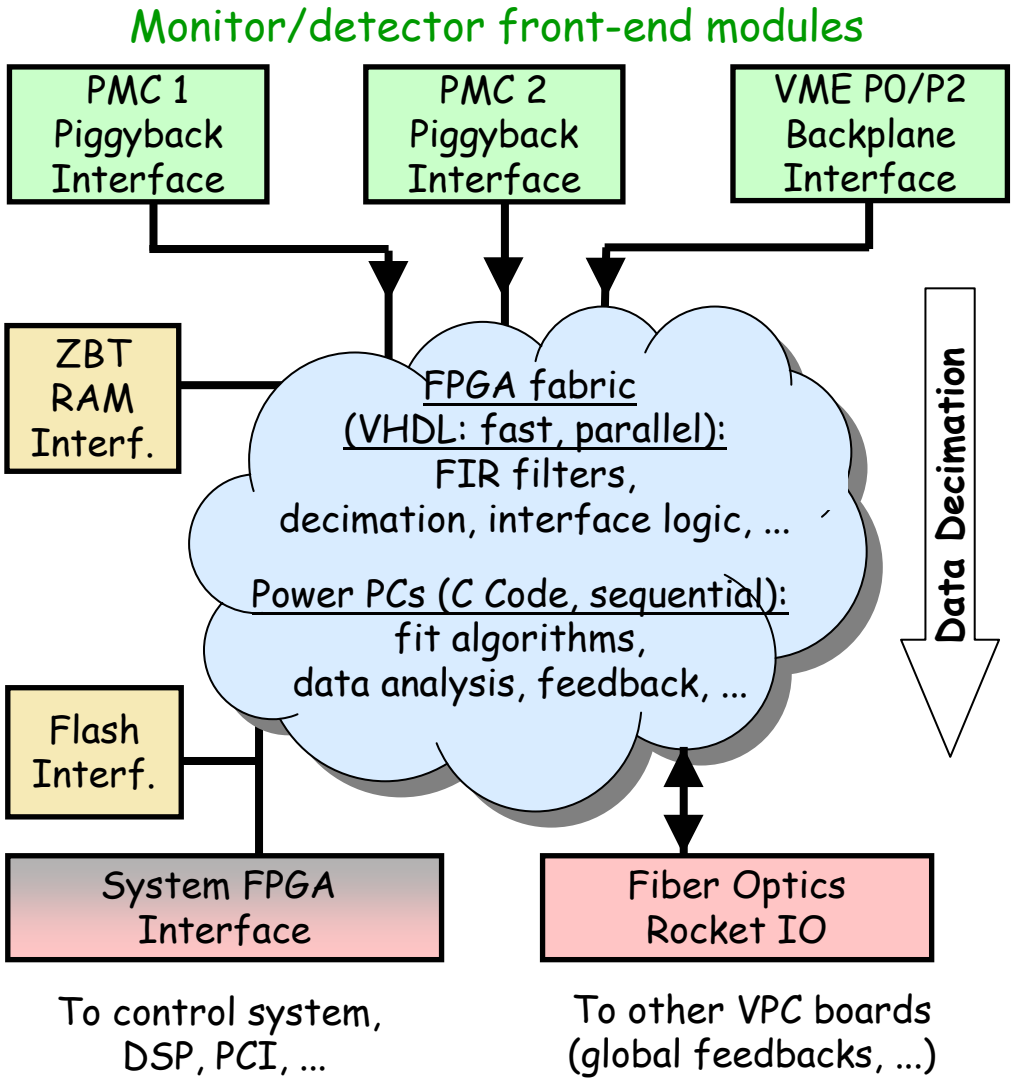
"VPC" Board Prototype



"System FPGA": Same Firmware for All Applications (VHDL)



"User FPGA" Firmware: Application-Dependent (DBPM, ...)



VPC Applications in PSI Diagnostics Section:

2004/2005

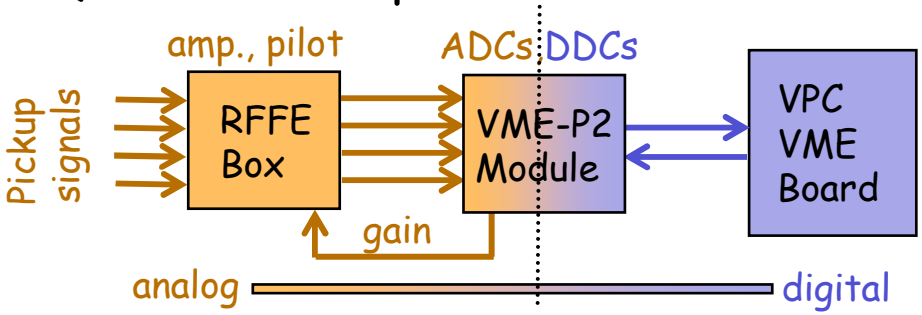
- Ring cyclotron upgrade: analog -> new digital proton BPMs
- PROSCAN proton therapy: beam profile/pos. measurement
- SLS: FOFB integration of new Photon BPM current digitizers
- SLS booster: DBPM1 gain control & readout (?)
- Test of 16-chan. 2-4 GSa/s waveform digitizer PMC ("Domino-Chip", PSI, S. Ritt)

Future (?)

- SLS FOFB and/or DBPM upgrade ? VPC upgrade ("VPC2") ?
- LEG, FEMTO, DESY-RF, ...

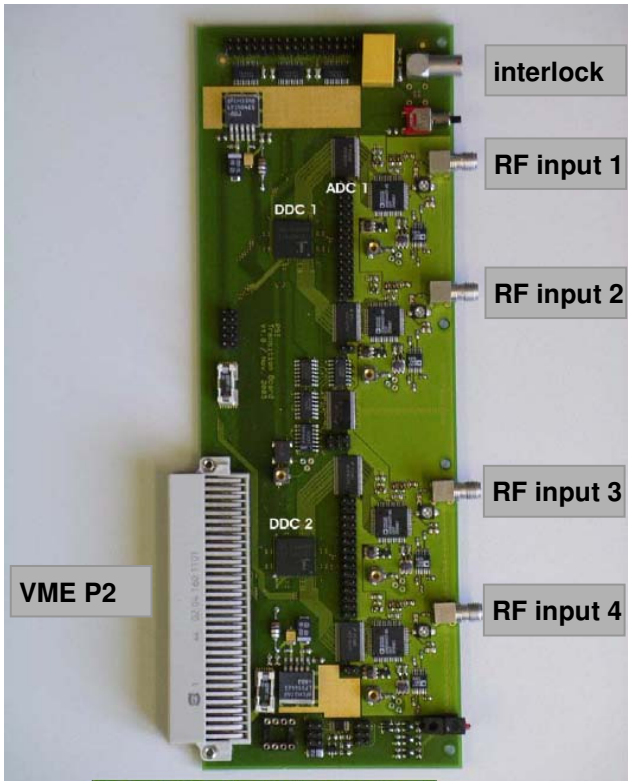
Proton DBPM: Hardware

- Motivation: more BPM bandwidth & dynamic range for PSI cyclotron transfer lines (want >10 kHz, >100 dB)
- RF front-end + VMEbus-P2 backplane module for VPC (PSI, P.-A.Duperrex, U. Mueller et al.)



- No mixer, direct (under-)sampling of 2nd RF harm. (101.26 MHz)
- RF frontend: filters, amplifiers, pilot (101.31 MHz)
- 4 ADCs, 2 DDC channels per ADC: pilot and beam signal simultaneously
- Beam signal normalized to pilot signal: Eliminates temperature drift, ...

VME-P2 Module



Proton DBPM: VPC "User FPGA" Firmw./Softw.

Safety-Relevant Functions: VHDL + C Code (PPC1)
(1 MW beam, proton therapy):

- Interface to VME-P2 backplane module (DDCs, ...)
- Beam position calculation & calibration
- Automatic gain control
- Interlock
- Additional filtering/decimation
- Time history
- ...

PPC2: (future) playground for physicists

- Data analysis, FFT, ...
- Change software (often) for machine shifts, ...
- ...

Modular FW design (CS-Interface, ...): re-use for PROSCAN beam profile monitor, ...

SLS: VPC for FOFB-Integration of Photon BPMs

New photon BPM current digitizer (Kramert GmbH)
- VME-P2 backplane module for VPC
- Programmable gain range (10E7)
- Max. 500 kSa/s
- Prototype: to be tested (2005)

VPC will provide:
- Photon BPM CS interface
- Gain control
- Averaging/filtering/calibration/data integrity checks/...
- Feedback links (2 GBaud fiber) to SLS FOFB:
  - "Libera-compatible" (?)
  - "Old" FOFB DSP boards get new gigabit-piggybacks
  - Protocol: DeltaNet (ring topology, token passing, data/trigger/sync., ...) ?

Future SLS FOFB/DBPM System ?

- Present FOFB/DBPM system running very well
- Will (hopefully) satisfy users for some years ...
- New system: development takes time -> start thinking now ...

Future SLS DBPMs: questions ...

- Single bunch resolution ? Noise ? When affordable ?
  - Atmel (now): 10 Bit, 2 GSa/s, 3 GHz
  - AD12500 (now): 12 Bit, 480 MSa/s, 460 MHz
- Averaging for 480 bunches in parallel (FPGA): TT+CO per bunch ?
- Fusion of FOFB and MBFB BPM electronics ?
- Commercial ("Libera(2)", ...) or in-house ("VPC2"+ PMC, ...) ?
- Temperature drift: Multiplexing ? Active temperature stabilization of analog BPM components (box: "ADC/Amplifier oven", 50±0.1 °C) ? Pos. calc. on RF side (SLS MBFB: hybrids) ? Normalize beam to pilot signal (coupled into beam pipe) ?
- Nonlinearities: assume single bunch resolution: "only" bunch charge dependence. 4->4 multiplexing ?
  Beam-based nonlinearity calibration & lookup-table ?
  Bunch pattern feedback & top-up sufficient ? Normalize to a pilot ?

VPC for Future SLS FOFB/DBPM System ?

Future SLS FOFB (my view ...):

- Likely: "intelligent" RF-BPMs (VPC2+PMC, Libera(2), ...), PBPMs, ... deliver beam pos., time stamp, ID, ... via 2-10 gigabit fiberlinks to one/more FOFB boards
- Fiberlinks: All BPM pos. + corrector currents to all FOFB boards, CRC checksums
- Fiberlink topology: Ring(s), some redundancy, flexible no. of BPMs & correctors
- FOFB boards (SVD alg., PID, ...):
  - Commercial (PPC-IOC + Fiberlink-PMC) or in-house (VPC or "VPC2", DSP/PPC) ? Matter of taste ...
  - One may be sufficient (@ 5-20 KHz corr. rate), several (distributed) may allow more flexibility & features
  - Corrector magnet PS: Direct connection to FOFB boards (via VME backplane, star/ring) – lower latency than VMEbus

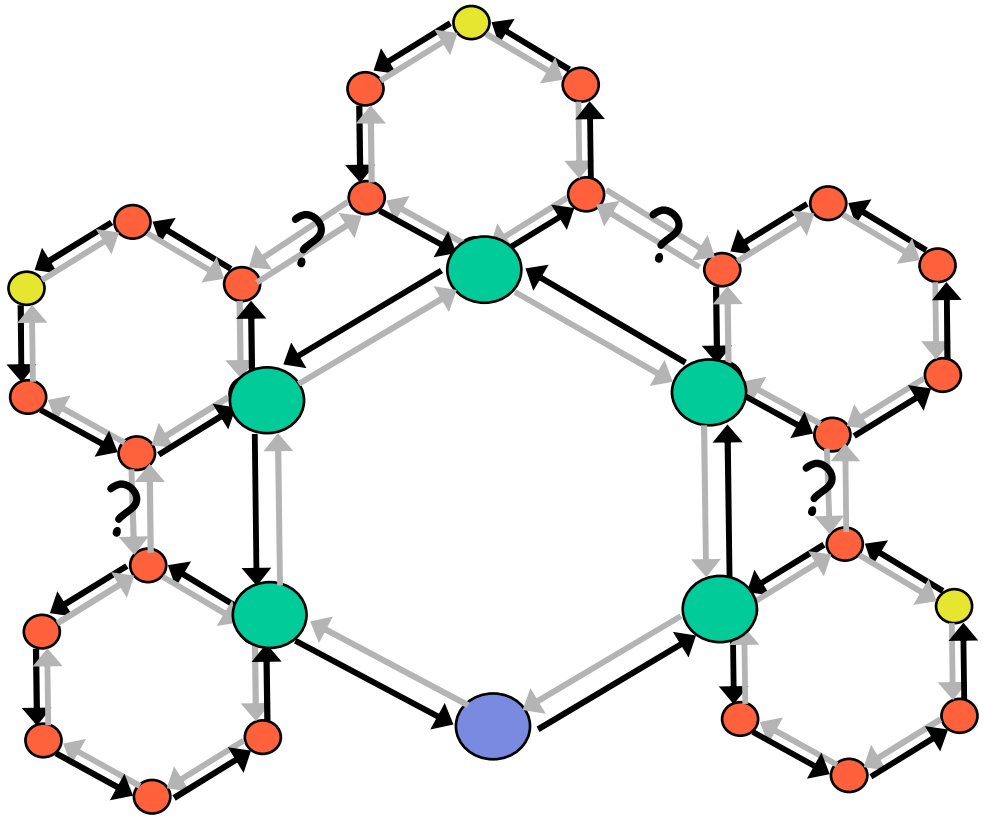
One Future Scenario (of Many ...):

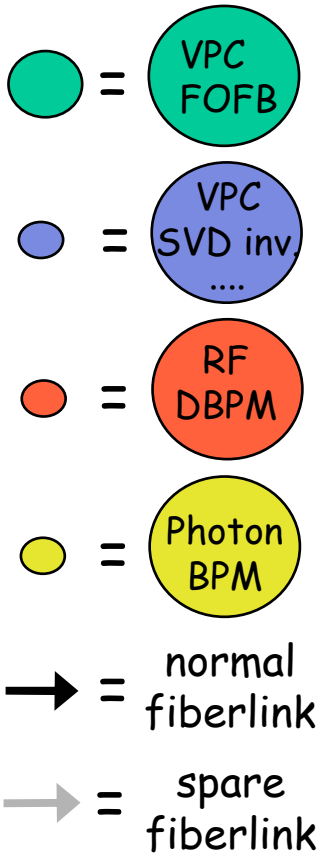
- VPC upgrade: Virtex4/5/..., better (no low-cost) DSP, 4-6 fiberlinks, 2-10 GBaud, 1 GB RAM
- New DBPMs: VPC + PMC. Single-bunch resolution (?)
- 12 VPC boards for FOFB (SVD alg. & PID)
- SVD inversion: 1 more VPC -> rapid low-level FOFB reconfiguration (BPM failures ...)
- HW-Migration from old to new SLS FOFB/DBPMs:
  - Change FOFB boards first ("Wiese DSP" -> VPC)
  - Connect DBPM1 boards (LVDS) to additional VPCs (temporarily, ~6 BPMs per VPC): fiberlink to FOFB boards, old BPMs look (nearly) like new ones (simultaneous turn-turn & closed orbit ...)
  - Replace old BPMs with new ones (incremental, less important ones first, test & compare)
  - Use SLS booster as FOFB testbed (?)

One Feasible FOFB Topology:

Only schematically, fewer sectors & BPMs than SLS ...:

- Token passing, package with BPM ID, CRC, time stamps, trig/sync... ?
- Tolerates 1 BPM failure per sub-ring
- FOFB board failures: rare & hot-swap ...





Conclusions

The VPC board:

- Saved/will save man power in several monitor projects by sharing common ("generic") HW/FW/SW
- May not be the final platform for the future SLS FOFB/DBPM system, but ...
- ... allows us to get experience with technology that is relevant for the future SLS FOFB/DBPM system, even if it should not be an in-house design but a commercial solution (or a mixture)
- Provides (some) building blocks (VHDL, ...) & knowledge for possible future projects (single-board MFBF ? ADC-FPGA-DAC ?)

Linux has been installed successfully on the User FPGA of the VPC (Gerd Teidel). But still no ports for TFT screen and joysticks :-(

Thank you for your attention, and ...
... I'm sure my time is up :-)