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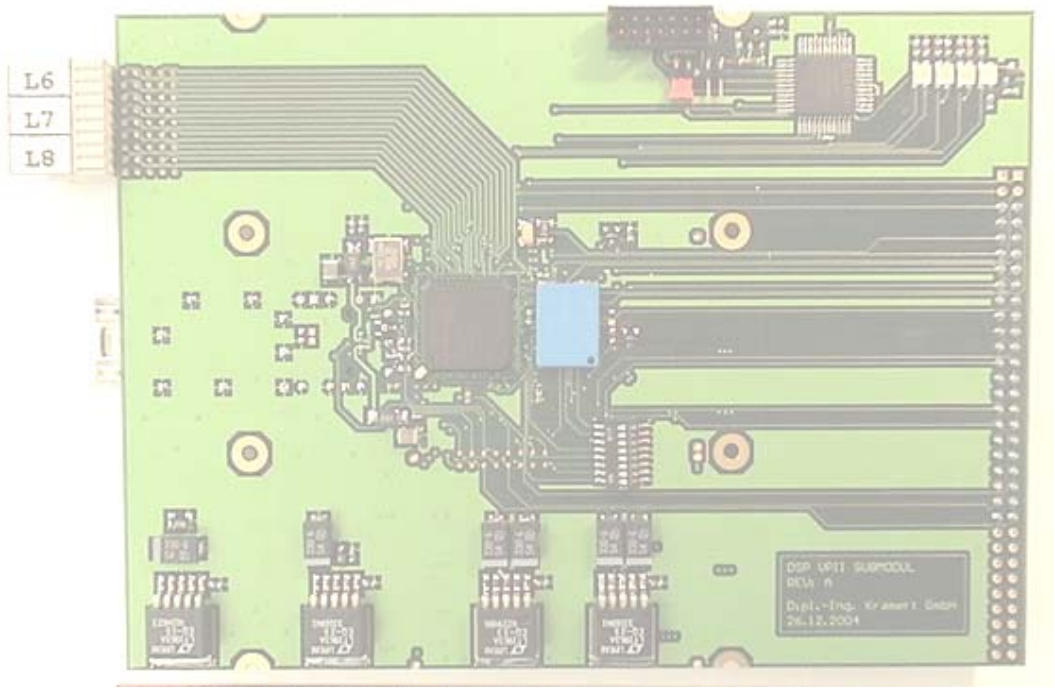
Instruction Manual

SHARC IO-Pack: DSP VPII



All technical data subject to change without notice.

1 Manual Revision History

Version	Date	Name	Comments
A	Feb. 10, 2005	R.Kramert	DSP_VPII_Submodul2.doc
B	Feb. 14, 2005	R.Kramert	DSP_VPII_Submodul3.doc
C	Sept. 8, 2005	R.Kramert	DSP_VPII_Submodul4.doc
D	Oct. 11, 2005	R.Kramert	DSP_VPII_Submodul5.doc
E	Oct. 18, 2005	R.Kramert	DSP_VPII_Submodul6.doc
F	Oct. 19, 2005	R.Kramert	DSP_VPII_Submodul7.doc
G	Mar. 21, 2006	R.Kramert	DSP_VPII_Submodul8.doc
H	Jan. 23, 2007	G.Marinkovic	DSP_VPII_Submodul9.doc

2 Contents

3 Glossary

SHARC IO-Pack	A piggy back concept which realizes a very flexible I/O configuration to the SHARC DSPs.
LCTL	Link Buffer Control Register
LCOM	Link Common Control Register
GCR	Gain Control Register
TCR	Temperature Control Register
BPM	Beam Position Monitor
pBPM	photon Beam Position Monitor
RF-FE	Radio Frequency Front End VME Module
WS-2126	VME Sharc Cluster Module
VPC	**V**ME **P**hysical-Mezzanine-Card **C**arrier Module
CD-704	Four Channel I/V-ADC VME Transition Module
TB-705A	Transition Board, located at the rear slot of each BPM-RF-Module and DSP-Module. The transition board is physically connected to the four temperature sensors and five gain-DACs of the front-RF-module. Communication between the transition boards is done via two serial RJ45 differential ports.

4 General Description

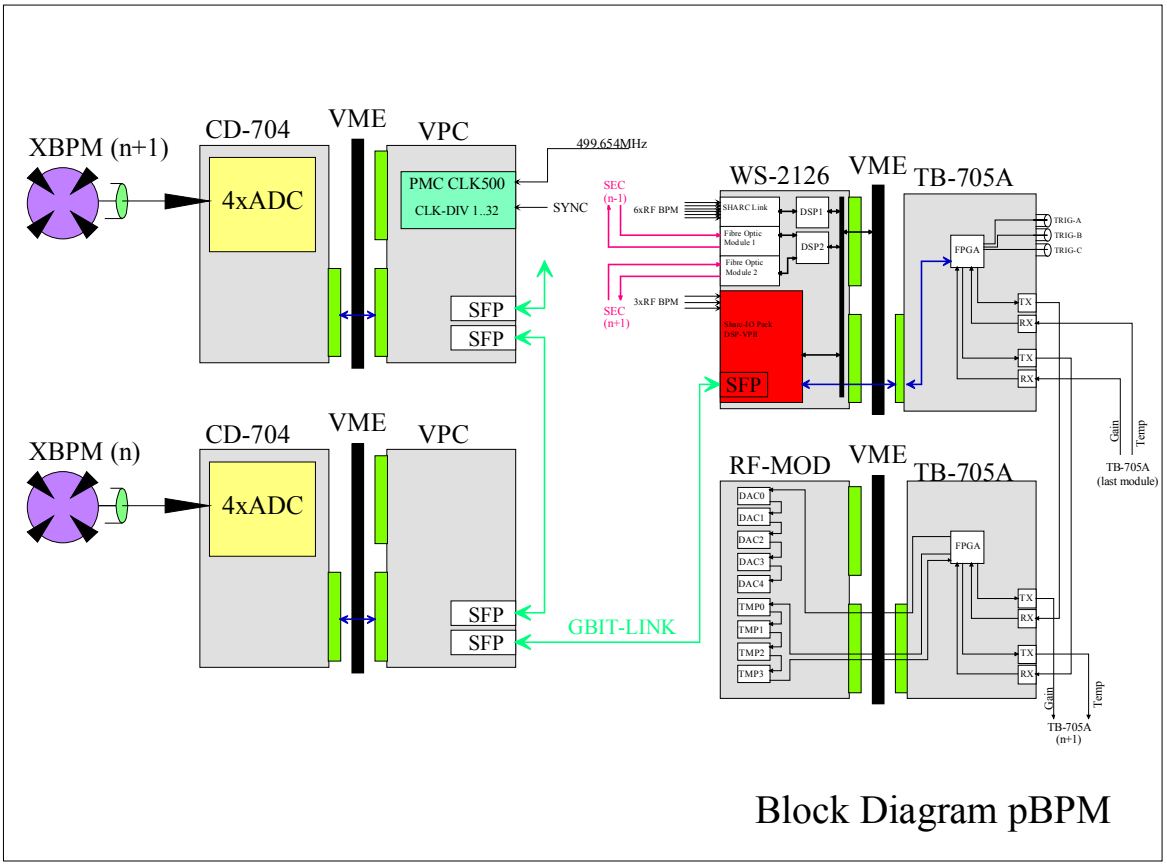


Table 1: SLS-pBPM SYSTEM

The DSP VPII Submodule is a size 3 Sharc IO-Pack. A Virtex II Pro FPGA realizes four communication tasks. Eight memory pages are available at base address (towards VME) 0x1400. Memory mapping is controlled by the Page-Select-Register PSR0 (0x3F). Page 0..4 are predefined IO-ports and related registers. Page 5..7 are not used.

The Gain Control Ports are extended to nine ports with five channels each and mapped to 0x00…0x2C on memory page 0. If an error occurs during link access then an error bit is set. These registers are physically located on the TB-705A transition board. There is write and read access to all gain registers.

There are 9x4 Temperature Sensors. These channels are mapped to 0x00…0x23 on memory page 1. The sensors are periodically read and the registers are updated once per second. These registers are physically located on the TB-705A transition board. There is read access to all Temp registers.

Three Sharc Link Ports are emulated with Link Buffer Control Register (LCTL), Link Common Control Register (LCOM) and three Link Buffer Fifos with a depth of two. These Ports work with 40 MHz at release 1 but are prepared to work with 80 MHz if needed in a later release. The Sharc Link Ports are mapped to memory page 2.

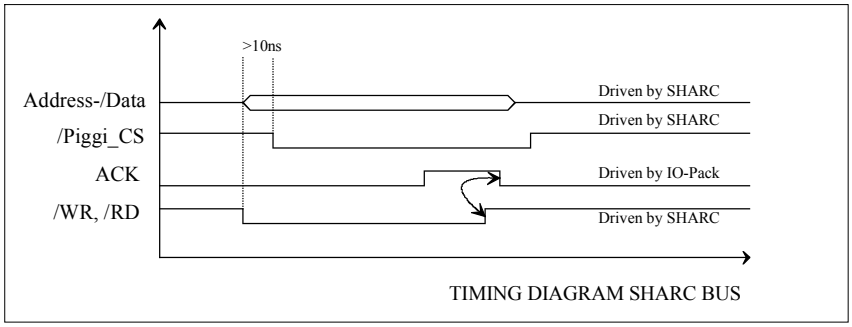
Memory is reserved and predefined for four p-BPM's on memory page 3.

Features:

- 3 Differential Sharc Link Port Emulation
- Access to 9x5 RF Gain Control Ports
- Access to 9x4 Temperature Sensor Ports
- 1 SFP Fiber Optic Transceiver for p-BPM Communication

5 Timing Specifications

5.1 Sharc IO-Pack:

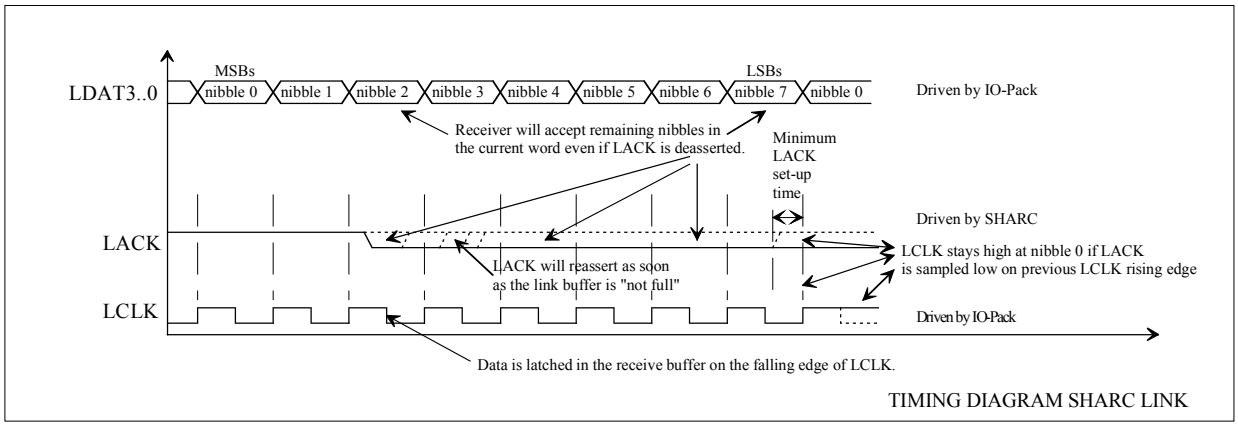


Address-decoding on the SHARC-IO Pack DSP VPII starts with a low level on /Piggi_CS. The IO-Pack logic asserts ACK high if:

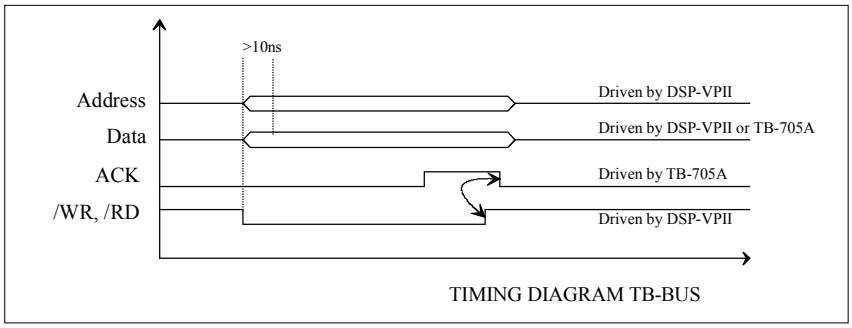
- On write cycles, it has captured the data
- On read cycles, it has submitted stable data on the data bus.

It is necessary to deassert ACK as fast as possible after /RD or /WR are invalid. The logic waits for /RD and /WR inactive and terminates activity.

5.2 Sharc Link:



5.3 Sharc-IO Pack DSP-VPII To Transition Board TB-705A:



Address-decoding on the Transition Board starts with a low level on /WR or /RD. The Transition Board logic asserts ACK high if:

- On write cycles, it has captured the data
- On read cycles, it has submitted stable data on the data bus.

It is necessary to deassert ACK as fast as possible after /RD or /WR are invalid. The logic waits for /RD and /WR inactive and terminates activity.

6 Address Map

Sharc IO-Pack5: local address base (VME) 0x1400, Databus SD[31:16] mapped to VME D[15:0]
Sharc IO-Pack6: local address base (VME) 0x1800, Databus SD[31:16] mapped to VME D[15:0] (not used)

Page 0: Range 0x00...0x3E (address mapping towards DSP side):

Resolution: DAC_{OUT} = 5V/(2^16) ≈ 76uV/Bit

Offset (Hex)	Bit [MSB-LSB]	Read/Write	Description
0x00	[15:0]	W	RF0, DAC0 RF-Gain
0x01	[15:0]	W	RF0, DAC1 RF-Gain
0x02	[15:0]	W	RF0, DAC2 RF-Gain
0x03	[15:0]	W	RF0, DAC3 RF-Gain
0x04	[15:0]	W	RF0, DAC4 RF-Gain
0x05	[15:0]	W	RF1, DAC0 RF-Gain
0x06	[15:0]	W	RF1, DAC1 RF-Gain
0x07	[15:0]	W	RF1, DAC2 RF-Gain
0x08	[15:0]	W	RF1, DAC3 RF-Gain
0x09	[15:0]	W	RF1, DAC4 RF-Gain
0x0A	[15:0]	W	RF2, DAC0 RF-Gain
0x0B	[15:0]	W	RF2, DAC1 RF-Gain
0x0C	[15:0]	W	RF2, DAC2 RF-Gain
0x0D	[15:0]	W	RF2, DAC3 RF-Gain
0x0E	[15:0]	W	RF2, DAC4 RF-Gain
0x0F	[15:0]	W	RF3, DAC0 RF-Gain
0x10	[15:0]	W	RF3, DAC1 RF-Gain
0x11	[15:0]	W	RF3, DAC2 RF-Gain
0x12	[15:0]	W	RF3, DAC3 RF-Gain
0x13	[15:0]	W	RF3, DAC4 RF-Gain
0x14	[15:0]	W	RF4, DAC0 RF-Gain
0x15	[15:0]	W	RF4, DAC1 RF-Gain
0x16	[15:0]	W	RF4, DAC2 RF-Gain
0x17	[15:0]	W	RF4, DAC3 RF-Gain
0x18	[15:0]	W	RF4, DAC4 RF-Gain
0x19	[15:0]	W	RF5, DAC0 RF-Gain
0x1A	[15:0]	W	RF5, DAC1 RF-Gain
0x1B	[15:0]	W	RF5, DAC2 RF-Gain
0x1C	[15:0]	W	RF5, DAC3 RF-Gain
0x1D	[15:0]	W	RF5, DAC4 RF-Gain
0x1E	[15:0]	W	RF6, DAC0 RF-Gain
0x1F	[15:0]	W	RF6, DAC1 RF-Gain
0x20	[15:0]	W	RF6, DAC2 RF-Gain
0x21	[15:0]	W	RF6, DAC3 RF-Gain
0x22	[15:0]	W	RF6, DAC4 RF-Gain
0x23	[15:0]	W	RF7, DAC0 RF-Gain
0x24	[15:0]	W	RF7, DAC1 RF-Gain
0x25	[15:0]	W	RF7, DAC2 RF-Gain
0x26	[15:0]	W	RF7, DAC3 RF-Gain
0x27	[15:0]	W	RF7, DAC4 RF-Gain
0x28	[15:0]	W	RF8, DAC0 RF-Gain
0x29	[15:0]	W	RF8, DAC1 RF-Gain
0x2A	[15:0]	W	RF8, DAC2 RF-Gain
0x2B	[15:0]	W	RF8, DAC3 RF-Gain
0x2C	[15:0]	W	RF8, DAC4 RF-Gain
0x2D...0x3E	[15:0]		Not used

Offset (Hex)	Bit [MSB-LSB]	Read/Write	Description
0x00	[15:0]	R	RF(number of TB-705 slaves - 9), DAC0 RF-Gain
0x01	[15:0]	R	RF(number of TB-705 slaves - 9), DAC1 RF-Gain
0x02	[15:0]	R	RF(number of TB-705 slaves - 9), DAC2 RF-Gain
0x03	[15:0]	R	RF(number of TB-705 slaves - 9), DAC3 RF-Gain
0x04	[15:0]	R	RF(number of TB-705 slaves - 9), DAC4 RF-Gain
0x05	[15:0]	R	RF(number of TB-705 slaves - 8), DAC0 RF-Gain
0x06	[15:0]	R	RF(number of TB-705 slaves - 8), DAC1 RF-Gain
0x07	[15:0]	R	RF(number of TB-705 slaves - 8), DAC2 RF-Gain
0x08	[15:0]	R	RF(number of TB-705 slaves - 8), DAC3 RF-Gain
0x09	[15:0]	R	RF(number of TB-705 slaves - 8), DAC4 RF-Gain
0x0A	[15:0]	R	RF(number of TB-705 slaves - 7), DAC0 RF-Gain
0x0B	[15:0]	R	RF(number of TB-705 slaves - 7), DAC1 RF-Gain
0x0C	[15:0]	R	RF(number of TB-705 slaves - 7), DAC2 RF-Gain
0x0D	[15:0]	R	RF(number of TB-705 slaves - 7), DAC3 RF-Gain
0x0E	[15:0]	R	RF(number of TB-705 slaves - 7), DAC4 RF-Gain
0x0F	[15:0]	R	RF(number of TB-705 slaves - 6), DAC0 RF-Gain
0x10	[15:0]	R	RF(number of TB-705 slaves - 6), DAC1 RF-Gain
0x11	[15:0]	R	RF(number of TB-705 slaves - 6), DAC2 RF-Gain
0x12	[15:0]	R	RF(number of TB-705 slaves - 6), DAC3 RF-Gain
0x13	[15:0]	R	RF(number of TB-705 slaves - 6), DAC4 RF-Gain
0x14	[15:0]	R	RF(number of TB-705 slaves - 5), DAC0 RF-Gain
0x15	[15:0]	R	RF(number of TB-705 slaves - 5), DAC1 RF-Gain
0x16	[15:0]	R	RF(number of TB-705 slaves - 5), DAC2 RF-Gain
0x17	[15:0]	R	RF(number of TB-705 slaves - 5), DAC3 RF-Gain
0x18	[15:0]	R	RF(number of TB-705 slaves - 5), DAC4 RF-Gain
0x19	[15:0]	R	RF(number of TB-705 slaves - 4), DAC0 RF-Gain
0x1A	[15:0]	R	RF(number of TB-705 slaves - 4), DAC1 RF-Gain
0x1B	[15:0]	R	RF(number of TB-705 slaves - 4), DAC2 RF-Gain
0x1C	[15:0]	R	RF(number of TB-705 slaves - 4), DAC3 RF-Gain
0x1D	[15:0]	R	RF(number of TB-705 slaves - 4), DAC4 RF-Gain
0x1E	[15:0]	R	RF(number of TB-705 slaves - 3), DAC0 RF-Gain
0x1F	[15:0]	R	RF(number of TB-705 slaves - 3), DAC1 RF-Gain
0x20	[15:0]	R	RF(number of TB-705 slaves - 3), DAC2 RF-Gain
0x21	[15:0]	R	RF(number of TB-705 slaves - 3), DAC3 RF-Gain
0x22	[15:0]	R	RF(number of TB-705 slaves - 3), DAC4 RF-Gain
0x23	[15:0]	R	RF(number of TB-705 slaves - 2), DAC0 RF-Gain
0x24	[15:0]	R	RF(number of TB-705 slaves - 2), DAC1 RF-Gain
0x25	[15:0]	R	RF(number of TB-705 slaves - 2), DAC2 RF-Gain
0x26	[15:0]	R	RF(number of TB-705 slaves - 2), DAC3 RF-Gain
0x27	[15:0]	R	RF(number of TB-705 slaves - 2), DAC4 RF-Gain
0x28	[15:0]	R	RF(number of TB-705 slaves - 1), DAC0 RF-Gain
0x29	[15:0]	R	RF(number of TB-705 slaves - 1), DAC1 RF-Gain
0x2A	[15:0]	R	RF(number of TB-705 slaves - 1), DAC2 RF-Gain
0x2B	[15:0]	R	RF(number of TB-705 slaves - 1), DAC3 RF-Gain
0x2C	[15:0]	R	RF(number of TB-705 slaves - 1), DAC4 RF-Gain
0x2D...0x3E	[15:0]		Not used

Please note: The data read is not necessarily the data written to this DAC but the data acknowledged by the corresponding TB-705 slave. The data position has an offset depending on how many TB-705 slaves are in the daisy chain.

Page 1: Range 0x00...0x3E (address mapping towards DSP side):

The temperature provided to the DSP is the value read from the LM-92 chip. This means it is 16bit wide containing:

- bit 0: low temperature flag (< 10°C),
- bit 1: high temperature flag (> 64°C),
- bit 2: critical temperature flag (> 80°C),
- bits 14-3: the temperature in 0.0625°C steps and
- bit 15: the sign bit of the temperature.

Offset (Hex)	Bit [MSB-LSB]	Read/Write	Description
0x00	[15:0]	R	RF(number of TB-705 slaves - 9), Temp Sensor 0
0x01	[15:0]	R	RF(number of TB-705 slaves - 9), Temp Sensor 1
0x02	[15:0]	R	RF(number of TB-705 slaves - 9), Temp Sensor 2
0x03	[15:0]	R	RF(number of TB-705 slaves - 9), Temp Sensor 3
0x04	[15:0]	R	RF(number of TB-705 slaves – 8), Temp Sensor 0
0x05	[15:0]	R	RF(number of TB-705 slaves – 8), Temp Sensor 1
0x06	[15:0]	R	RF(number of TB-705 slaves – 8), Temp Sensor 2
0x07	[15:0]	R	RF(number of TB-705 slaves – 8), Temp Sensor 3
0x08	[15:0]	R	RF(number of TB-705 slaves – 7), Temp Sensor 0
0x09	[15:0]	R	RF(number of TB-705 slaves – 7), Temp Sensor 1
0x0A	[15:0]	R	RF(number of TB-705 slaves – 7), Temp Sensor 2
0x0B	[15:0]	R	RF(number of TB-705 slaves – 7), Temp Sensor 3
0x0C	[15:0]	R	RF(number of TB-705 slaves – 6), Temp Sensor 0
0x0D	[15:0]	R	RF(number of TB-705 slaves – 6), Temp Sensor 1
0x0E	[15:0]	R	RF(number of TB-705 slaves – 6),Temp Sensor 2
0x0F	[15:0]	R	RF(number of TB-705 slaves – 6), Temp Sensor 3
0x10	[15:0]	R	RF(number of TB-705 slaves – 5), Temp Sensor 0
0x11	[15:0]	R	RF(number of TB-705 slaves – 5), Temp Sensor 1
0x12	[15:0]	R	RF(number of TB-705 slaves – 5), Temp Sensor 2
0x13	[15:0]	R	RF(number of TB-705 slaves – 5), Temp Sensor 3
0x14	[15:0]	R	RF(number of TB-705 slaves – 4), Temp Sensor 0
0x15	[15:0]	R	RF(number of TB-705 slaves – 4), Temp Sensor 1
0x16	[15:0]	R	RF(number of TB-705 slaves – 4), Temp Sensor 2
0x17	[15:0]	R	RF(number of TB-705 slaves – 4), Temp Sensor 3
0x18	[15:0]	R	RF(number of TB-705 slaves – 3), Temp Sensor 0
0x19	[15:0]	R	RF(number of TB-705 slaves – 3), Temp Sensor 1
0x1A	[15:0]	R	RF(number of TB-705 slaves – 3), Temp Sensor 2
0x1B	[15:0]	R	RF(number of TB-705 slaves – 3), Temp Sensor 3
0x1C	[15:0]	R	RF(number of TB-705 slaves – 2), Temp Sensor 0
0x1D	[15:0]	R	RF(number of TB-705 slaves – 2), Temp Sensor 1
0x1E	[15:0]	R	RF(number of TB-705 slaves – 2), Temp Sensor 2
0x1F	[15:0]	R	RF(number of TB-705 slaves – 2), Temp Sensor 3
0x20	[15:0]	R	RF(number of TB-705 slaves – 1), Temp Sensor 0
0x21	[15:0]	R	RF(number of TB-705 slaves – 1), Temp Sensor 1
0x22	[15:0]	R	RF(number of TB-705 slaves – 1), Temp Sensor 2
0x23	[15:0]	R	RF(number of TB-705 slaves – 1), Temp Sensor 3
0x24...0x3E	[15:0]		Not used

Please note: The data position has an offset depending on how many TB-705 slaves are in the daisy chain.

Page 2: (address mapping towards DSP side):

Offset (Hex)	Bit [MSB-LSB]	Read/Write	Description
0x00	[15:0]	R	Link Buffer FIFO 0 Low Word
0x01	[15:0]	R	Link Buffer FIFO 0 High Word
0x02	[15:0]	R	Link Buffer FIFO 1 Low Word
0x03	[15:0]	R	Link Buffer FIFO 1 High Word
0x04	[15:0]	R	Link Buffer FIFO 2 Low Word
0x05	[15:0]	R	Link Buffer FIFO 2 High Word
0x06	[15:0]	R/W	Link Buffer Control Register (LCTL)
0x07	[15:0]	R/W	Link Common Control Register (LCOM)
0x08..0x3E			not used

Page 3: (address mapping towards DSP side):

Offset (Hex)	Bit [MSB-LSB]	Read/Write	Description
0x00	[15:0]	R	X pBPM 0 Low Word
0x01	[15:0]	R	X pBPM 0 High Word
0x02	[15:0]	R	Y pBPM 0 Low Word
0x03	[15:0]	R	Y pBPM 0 High Word
0x04	[15:0]	R	Intensity pBPM 0 Low Word
0x05	[15:0]	R	Intensity pBPM 0 High Word
0x06	[15:0]	R	Status pBPM 0
0x07	[15:0]	R	Event Counter pBPM 0
0x08	[15:0]	R	X pBPM 1 Low Word
0x09	[15:0]	R	X pBPM 1 High Word
0x0A	[15:0]	R	Y pBPM 1 Low Word
0x0B	[15:0]	R	Y pBPM 1 High Word
0x0C	[15:0]	R	Intensity pBPM 1 Low Word
0x0D	[15:0]	R	Intensity pBPM 1 High Word
0x0E	[15:0]	R	Status pBPM 1
0x0F	[15:0]	R	Event Counter pBPM 1
0x10	[15:0]	R	X pBPM 2 Low Word
0x11	[15:0]	R	X pBPM 2 High Word
0x12	[15:0]	R	Y pBPM 2 Low Word
0x13	[15:0]	R	Y pBPM 2 High Word
0x14	[15:0]	R	Intensity pBPM 2 Low Word
0x15	[15:0]	R	Intensity pBPM 2 High Word
0x16	[15:0]	R	Status pBPM 2
0x17	[15:0]	R	Event Counter pBPM 2
0x18	[15:0]	R	X pBPM 3 Low Word
0x19	[15:0]	R	X pBPM 3 High Word
0x1A	[15:0]	R	Y pBPM 3 Low Word
0x1B	[15:0]	R	Y pBPM 3 High Word
0x1C	[15:0]	R	Intensity pBPM 3 Low Word
0x1D	[15:0]	R	Intensity pBPM 3 High Word
0x1E	[15:0]	R	Status pBPM 3
0x1F	[15:0]	R	Event Counter pBPM 3
0x20..0x3E			not used

Page 4: Range 0x00...0x3E (address mapping towards DSP side):

Offset (Hex)	Bit [MSB-LSB]	Read/Write	Description
0x00	[15:0]	R	Free running counter with a resolution of 12.5ns
0x01	[15:0]	R/W	Link error counter. Writing to this address resets the counter to 0.
0x02...03E	[15:0]		Not used

Page 5..7: not used

7 Registers

7.1 Page-Select-Register at location (0x3F):

Bit 2,1,0	Definition
0x0	Map Memory Page 0
0x1	Map Memory Page 1
0x2	Map Memory Page 2
0x3	Map Memory Page 3
0x4	Map Memory Page 4
0x5	Map Memory Page 5
0x6	Map Memory Page 6
0x7	Map Memory Page 7

7.2 Link Buffer FIFOx
Location : 0x00..0x14, Page2

In general, after reading a FIFO, the FIFO is shifted and the new value is present at the FIFO output. Here, this is true only for the low word register of the Link Buffer FIFO. So when reading the FIFO, start with the high word register first and then continue with the low word register. After reading the low word register, both high and low registers are shifted.

7.3 Link Buffer Control Register LCTL
Location : 0x18, Page2

Bit #	Name	Function
0..3	*	Link Buffer 0 Control
4..7	*	Link Buffer 1 Control
8..11	*	Link Buffer 2 Control
12..15	*	reserved

Table 7.3: Link Control Register (LCTL)
* Each four-bit group includes the following control bits for each link buffer. (x=0,1,2)

Bit #	Name	Definition
0+4x	LxEN	LBUFx enable
1+4x	LxTRAN	LBUFx direction: 1 = transmit, 0 = receive
2+4x	LEXTx	Extended Word size: 1 = 48 bit transfers, 0 = 32 bit transfers
1+4x	*	reserved

LCTL Control Bits:

LxEN — Enables a link buffer. As a buffer is disabled (LxEN transition from high to low), the LxSTAT and LRERR bits are cleared. When its buffer is disabled, an assigned link port stops receiving (driving LxACK) or transmitting (driving LxCLK). To pull the LxACK and LxCLK signals low, enable the pull down resistors with the LCOM register.

LxTRAN — **Gives** the direction of the link buffer and link port: 0 to receive link data, 1 to transmit link data

LEXTx — **Gives** the size of the link buffer, link port and data transfer through the Link port: 1 = 48 bit transfer, 0 = 32 bit transfer

7.4 Link Common Control Register LCOM
Location : 0x1C, Page2

Bit #	Name	Function
[0..1]	L0STAT(0:1)	Link Buffer 0 status: 11 = full, 00 = empty, 10 = one word *
[2..3]	L1STAT(0:1)	Link Buffer 1 status: 11 = full, 00 = empty, 10 = one word *
[4..5]	L2STAT(0:1)	Link Buffer 2 status: 11 = full, 00 = empty, 10 = one word *
6	LCLKX20	Transfer data at 2x the clock rate on Link Buffer 0
7	LCLKX21	Transfer data at 2x the clock rate on Link Buffer 1
8	LCLKX22	Transfer data at 2x the clock rate on Link Buffer 2
9	LRERR0	Receive pack error status for Link Buffer 0
10	LRERR1	Receive pack error status for Link Buffer 1
11	LRERR2	Receive pack error status for Link Buffer 2
[12..15]	reserved	

Table 7.4: Common Control Register (LCOM)
* The code 01 does not appear as a valid status

LCOM Control Bits:

LxSTAT(0:1) When transmitting, these status bits indicate whether there is room in the buffer for more data. When receiving, these status bits indicate whether new (unread) data is available in the receive buffer.
LxSTAT(1)=1 if there is data in the buffer. LxSTAT(0) =0 if there is room in the buffer. These bits are read-only. They are cleared when LxEN changes from 1 to 0. They may subsequently change state when the data buffer is read or written.

LCLKX2x This specifies link buffers to transfer at twice the ADSP-2106x clock frequency, and receive transfers occur at (up to) the ADSP-2106x clock frequency.

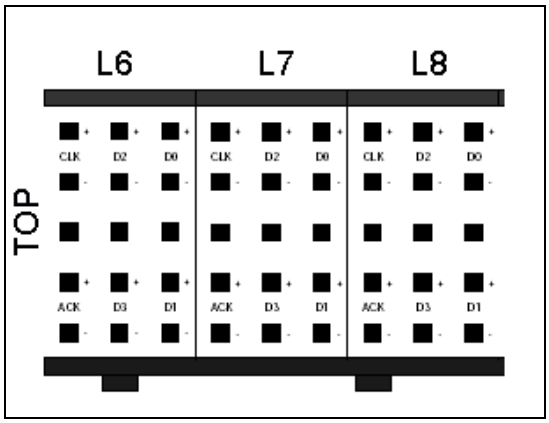
LRERRx These bits reflects the status of the receive nibble packer for each link buffer. LRERRx will equal 0 when the nibble packer is set to start receiving a new word. Otherwise it will be 1. If this bit is equal to 1 after a word is received, then an error has occurred (e.g. clock glitch). The LRERRx bits are cleared when LxEN changes from 1 to 0. They may subsequently change state when the link buffer is read or written or while a word is being received.

7.5 pBPM Register
Location : 0x00..0xF8, Page3
These memory locations are predefined and reserved for later use.

8 Connector Pin Specifications

8.1 Connector SharcLink Port J1:

This connector is a modified 2mm Z-Pack system. Each Link channel use 12 differential plus 3 shielded pins. Each differential pair has its own cable shield.



8.2 SFP Optical Transceiver Port:

This port is equipped with a HFBR 5720AL module. It is connected to the Virtex II Pro Multi Gigabit Transceiver Port 6. Its transfer rate is either 1062.5 MHz or 2125 MHz. Clock base is 106.25 MHz.

8.3Connector VME P2 Rear:

Pin	Name	Definition	I/O	Pin	Name	Definition	I/O
1A	Spare C	not used		1C	Spare A	not used	
2A	Spare D	not used		2C	Spare B	not used	
3A	TB-D0		I/O	3C	TB-A0	Transition Board Addressbus	O
4A	TB-D1	"	I/O	4C	TB-A1	"	O
5A	TB-D2	"	I/O	5C	TB-A2	"	O
6A	TB-D3	"	I/O	6C	TB-A3	"	O
7A	TB-D4	"	I/O	7C	TB-A4	"	O
8A	TB-D5	"	I/O	8C	TB-A5	"	O
9A	TB-D6	"	I/O	9C	TB-A6	"	O
10A	TB-D7	"	I/O	10C	TB-A7	"	O
11A	TB-D8	"	I/O	11C	TB-A8	"	O
12A	TB-D9	"	I/O	12C	TB-RDn	Read Strobe	O
13A	TB-D10	"	I/O	13C	TB-WRn	Write Strobe	O
14A	TB-D11	"	I/O	14C	TB-ACK	Acknowledge	I
15A	TB-D12	"	I/O	15C	TB-TRIG A	TB-Trigger Bus A for Sharc I/O-Pack	I/O
16A	TB-D13	"	I/O	16C	TB-TRIG B	TB-Trigger Bus B for Sharc I/O-Pack	I/O
17A	TB-D14	"	I/O	17C	TB-TRIG C	TB-Trigger Bus C for Sharc I/O-Pack	I/O
18A	DSP_SCLK	Sharc-Bus Clock 40 MHz	I/O	18C			
19A				19C			
20A				20C			
21A				21C			
22A	TB-D15	Transition Board Databus		22C	TB-A9	Transition Board Addressbus	
23A	Spare 2	not used		23C	Spare 4	not used	O
24A				24C			
25A				25C			
26A				26C			
27A				27C			
28A				28C			
29A				29C			
30A				30C			
31A				31C			

8.4 Connector Mezzanine J8 Sharc IO-Pack 5 Rear:

Pin-Nr.	Signal	Description
1	SA0	SHARC address bus (VME:A2)
3	SA1	SHARC address bus (VME:A5)
5	SA2	SHARC address bus (VME:A4)
9	DGND	
13	DGND	
15	SD17	SHARC data bus (VME:D1)
17	SD16	SHARC data bus (VME:D0)
29	+5VD	
31	/RD	Memory Read Strobe
43	SD20	SHARC data bus (VME:D4)
45	SD30	SHARC data bus (VME:D14)
47	SD28	SHARC data bus (VME:D12)
49	SD26	SHARC data bus (VME:D10)
51	SD24	SHARC data bus (VME:D8)
55	SD22	SHARC data bus (VME:D6)
57	SD21	SHARC data bus (VME:D5)
59	SD19	SHARC data bus (VME:D3)

Pin	Signal	Description
2	SA3	SHARC address bus (VME:A5)
4	SA4	SHARC address bus (VME:A6)
6	SA5	SHARC address bus (VME:A7)
8	+5VD	
10	DGND	
14	ACK	Memory Acknowledge
18	DGND	
22	PIGGY_CS 5	SHARC I/O-Pack Chipselect
30	SD18	SHARC data bus (VME:D2)
34	/WR	Memory Write Strobe
40	SCLK	System Clock (40MHz)
46	SD31	SHARC data bus (VME:D15)
48	SD29	SHARC data bus (VME:D13)
50	SD27	SHARC data bus (VME:D11)
52	SD25	SHARC data bus (VME:D9)
54	SD23	SHARC data bus (VME:D7)

8.5 Connector Mezzanine J9 Sharc IO-Pack 6 Rear:

Pin-Nr.	Signal	Description
9	DGND	
13	DGND	
29	+5VD	

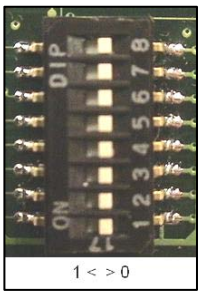
Pin	Signal	Description
8	+5VD	
10	DGND	
18	DGND	
22	PIGGY_CS 6	SHARC I/O-Pack Chipselect

8.6 Connector Mezzanine J10 Sharc IO-Pack 6 Front:

Pin-Nr.	Signal	Description
9	/RST	Board Hardware Reset
15	DGND	
23	DGND	
31	DGND	
47	DGND	
63	TRIGB	Trigger Bus B for SHARC I/O-Pack

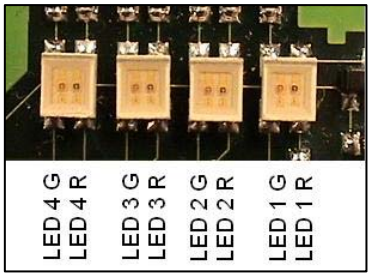
Pin	Signal	Description
2	TRIGC	Trigger Bus C for SHARC I/O-Pack
4	DGND	
48	DGND	
62	DGND	
64	TRIGA	Trigger Bus A for SHARC I/O-Pack

9 Switches



SW-1 not used
SW-2 not used
SW-3 not used
SW-4 not used
SW-5 not used
SW-6 not used
SW-7 not used
SW-8 not used

10 LEDs



LED 4 G	not used
LED 4 R	not used
LED 3 G	not used
LED 3 R	not used
LED 2 G	not used
LED 2 R	not used
LED 1 G	not used
LED 1 R	FPGA programmed

11 Power Requirements

Approx 0.9A at +5V