SLS DBPM Project
Fiber Optical Link module
and Firmware Documentation

Inhalt des Dokumentes

Beschreibung des Ersatzmoduls für das WS9003:
Fiber Optical Link module (FOL):

Dieses Dokument beschreibt die Funktionalität und Implementierungsdetails der Firmware für das Aufsteckmodule FOLSHARC_DIO. Es ersetzt jeweils zwei der bisher eingesetzten WS9003 Module.
Die Hauptfunktionalität besteht darin zwei SHARC DSP Prozessorbasisplatinen via DSP SHARC Link Ports mit einem SHARC DSP Prozessor über grössere Distanz zu verbinden. Dazu wird je eine SHARC DSP Basisplatine mit zwei Glasfaser Sende- und Empfangsmodulen (FOL) ausgestattet, welche jeweils durch eine Sende- und eine Empfangs Glasfaser mit dem benachbarten Module verbunden ist.
Neben der Basisfunktionalität des SHARC Link sind einige Konfigurationsregister und Statusregister über einen Adress- und Datenbus zugreifbar.

Abstract:

Description of the replacement module for the WS9003:
Fiber Optical Link Module (FOL):

This document describes the functionality and implementation details of the firmware for the piggyback FOLSHARC_DIO module. It is a replacement for two of the so far engaged Wiese WS9003 FOL modules. For that purpose each SHARC DSP main board is equipped with two transmit and receive Fiber Optical Link (FOL) modules, each is connected with a FOL module to the adjacent DSP main board.
Besides the basic functionality of the SHARC Link some Configuration and Status Register are accessible by the SHARC Processor module via a memory mapped device in addition.

Directory

1 Functional Overview Hardware:

The actual hardware set up in the SLS consists of several via Fiber connected WS 2126 base boards. Each of these boards has a receiver (RX) and a transmitter (TX) module (WS9003) to each of two adjacent WS2126 boards. The main functionality is to exchange compensation data for field stabilization within the SLS.

1.1 Older realization within the SLS with Wiese WS9003 modules:

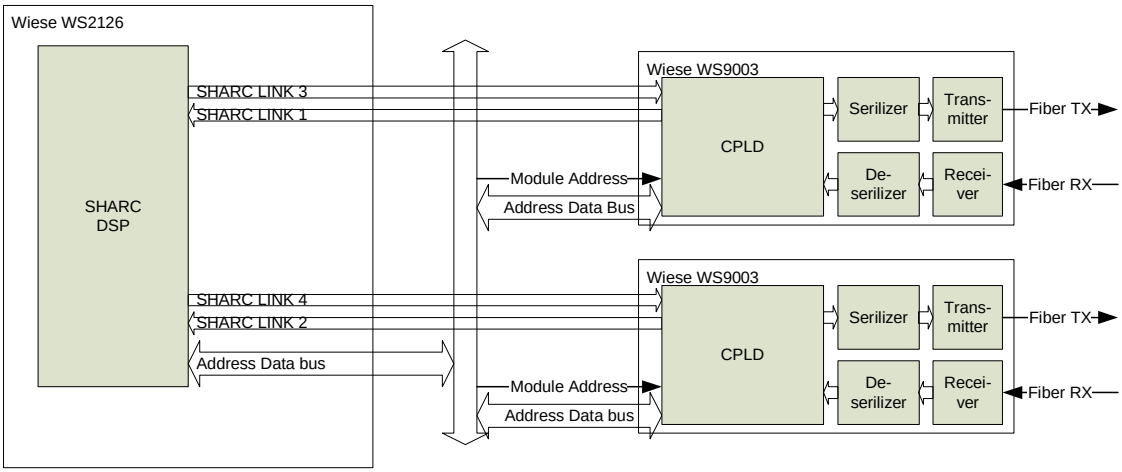

Figure 1: WS2126 with two Wiese WS9003 modules

1.2 New realization within the SLS with FOLSHARC_DIO modules:

Hardware differences to the Wiese WS 9003:
The Functionality of the serializer and deserializer in the Wiese 9003 is now realized within the FPGA shown in Figure 2.

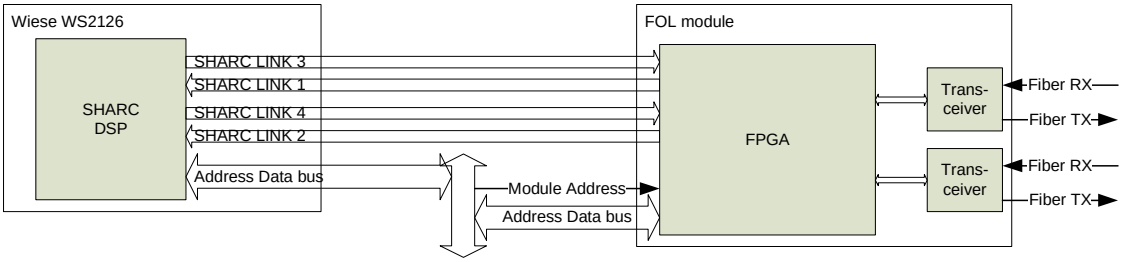

Figure 2: WS2126 with one FOL replacement module

1.3 Software differences:

The memory mapping of the newer combined module differs from the two original WS 9003 modules, because the two modules had separate address lines on each connector on the base board. Now only one connector is used causing a change in memory map. Details are presented in the memory bus section within this document.

2 Functional Overview FPGA

The fiber optical link module (FOL) is connected to a SHARC DSP Processor and two adjacent FOL modules, each with receiver and transmitter fiber. This allows to electrical connect the local SHARC DSP Processor to two adjacent SHARC DSP Processors via receiver and transmitter fiber of each module.
The fiber optical link module has a memory mapped connection to the SHARC DSP on the Wiese WS2126 baseboard. This interface is used for configuration and status requests.
The main task of this hardware module is connecting this SHARC DSP to two adjacent SHARC DSP modules via bidirectional fiber links. (1xRX fiber and 1xTX fiber)
The DSP communicates via two SHARC link port interfaces with the FPGA. The FPGA receives data on one of the two receiver link ports and transmits the data to the transmitter fiber link. If data is received from the fiber this data will be transmitted to on one of the two DSP transmitter link ports.

2.1 Firmware structural design

The firmware consists of several sub modules:

Module	Description
Top Level	This module defines electrical characteristics for the input and output pins. It was generated to abstract from the FPGA pin names.
Main	This module is used to group the IO pins to special functional sections. It decouples into several blocks.
System Clock Distribution	This is the main system clock distribution of the FPGA firmware. See clock domain section for details.
PLL 20MHz 40MHz, 80MHz	This module is used to generate a 40 MHz and an 80 MHz system clock from the external 20 MHz oscillator. The 40 MHz clock is used for the electrical compensation of the gigabit transceiver instance within the FPGA. The 80 MHz clock is used for configuration of the external reference oscillator that is needed for the gigabit transceiver block module.
PLL DSP	This module is used to synchronize the external system clock to the FPGA. It secures stable operation of the FSM within the FPGA.
Clock Configuration	This module configures the external reference oscillator. It reads the configuration via I2C and modifies them to have 83.333 MHz System clock frequency that feeds the GXB PLL within the FPGA. Comment: Each device has unique frequency parameters, so the current configuration has to be read from the external device before configuring.
I2C Link	This module is used for the readout and rewrite of the control and status registers of the external reference oscillator.
Configuration Registers	This is a slave device implementation of the memory mapped port of the SHARC DSP.

Media Converter	This module is used to transfer the received data from a SHARC DSP, received via the link port, to the gigabit transceiver and vice versa. The Fiber Optical Link protocol is also implemented within this Media Converter Module. Data is read and transferred to clock decoupling FIFO blocks. This module controls the sync word generation.
DSP to System	This module is the implementation of the data transfer module of the SHARC DSP to the FPGA internal FIFO blocks. Data from the DSP is transferred Nibble by Nibble. 32 Bits are marked as DSP Data word and stored within FIFO blocks.
System to DSP	This module writes data to a SHARC DSP via SHARC Link Port one or two. Data is read from a receiver FIFO of the GXB module RX0 or RX1.
GXB Transceiver	This module decouples the GXB from the media converter instance. The electrical compensation parameters are requested from this instance.
GXB	This module is used to implement the data transfer via gigabit transceiver module to and from FIBER. Resynchronization for bytes and double bytes is implemented here.
GXB Calibration	This module is used to calibrate the electrical parameters of the gigabit transceiver module.
Trigger to IRQ2, Error to IRQ1	This module drives the interrupt signals to the SHARC DSP. One selected trigger input is observed. When trigger occurs the SHARC DSP gets an interrupt request on IRQ2. When an error condition event occurs the SHARC DSP gets an interrupt request on IRQ1.
Package: Types	This is a package that contains the bus types that are used within the FOL firmware.

Table 1: Firmware Modules

2.2 Implemented Clock Domains

The Fiber optical link module consists of two fiber optical receivers and transmitters. These transmitters are served by 8B10B protocol. The high speed data serializer and deserializer (SERDES) circuitry is realized within the FPGA. A serial data rate of 1.5 gigabits per second is configured as link speed. This speed is near the bandwidth of the fiber transceiver diodes. The transfer data rate on the Fiber link is therefore 1.2 gigabits per second for each transmitter and receiver combination. Within the FPGA FIFO blocks are used to decouple from the external Clock Domains of SHARC DSP and receiver fiber link. Data is transferred internally with several 75 MHz clock distribution networks that drive the pipelined registered design. One mayor system clock domain oscillates synchronous to the transmitter clock domain and is used to transfer data from and to the connected SHARC DSP processor FIFO blocks. The usage of these clocks is mentioned in this section.

2.2.1 Clock domain Overview

The following figure is an overview of the implemented clock domain generation module.

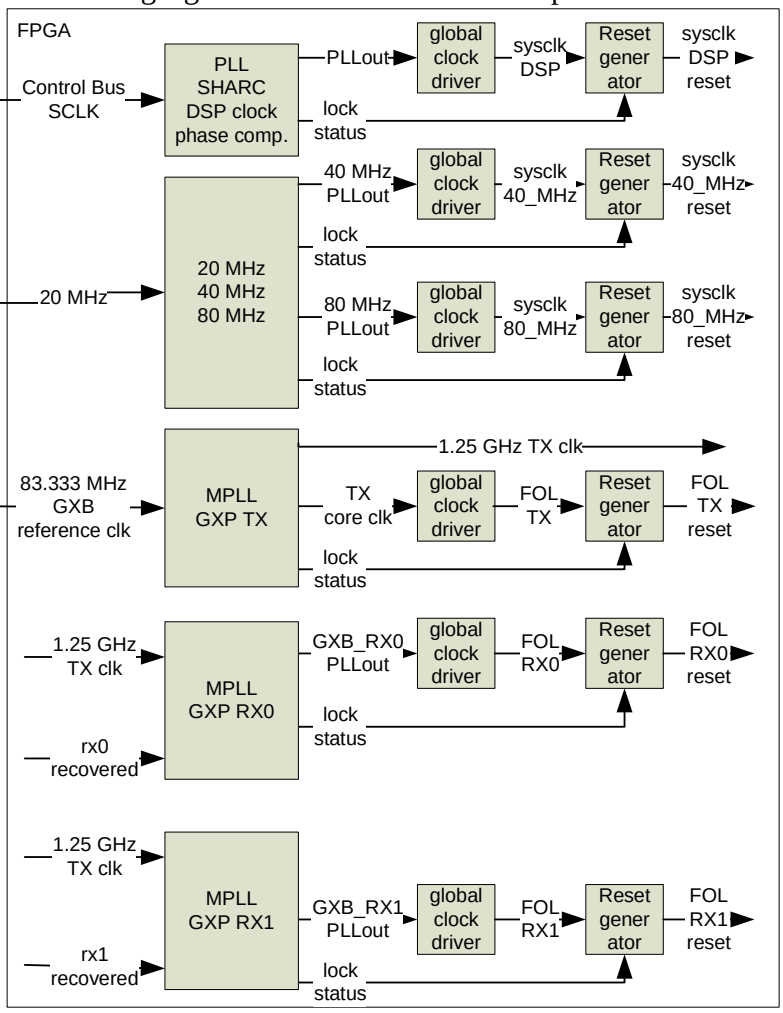

Figure 3: Clock domain driver Overview

2.2.2 Startup clock for system initialization

The external 20 MHz oscillator is used to configure the on board Reference Oscillator for the GXB transceiver on the one hand and to compensate for electrical and thermal variations of the GXB transceiver blocks within the FPGA on the other hand. The Figure 4 shows the clock domain distribution of the 20 MHz oscillator with the connected PLL that generates internal FPGA clock domain distribution for configuration and calibration.

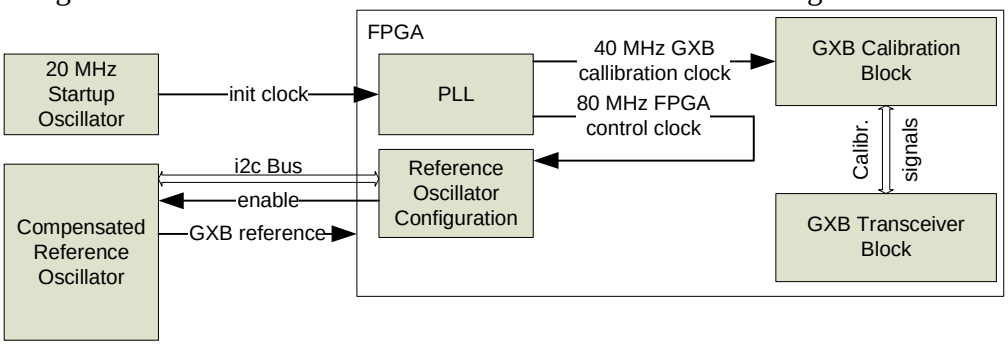

Figure 4: Startup Clock Domains and reference configuration block

The external 20 MHz oscillator is connected to an FPGA internal PLL to reach the frequency range of the GXB calibration block by doubling the external clock frequency to 40 MHz. The calibration block for the GXB transceivers is used to achieve stabilized operating conditions for the high speed clock signals within the FPGAs transceiver module.
The Reference Oscillator Configuration module is connected to the 20 MHz multiplied by four output of the PLL. The PLL also ensures the correct function of the logic implementation by observing the locked status of the PLL. At system startup the configuration registers of the reference oscillator are read and rewritten with the new configuration values. After Startup the GXB reference clock is programmed to 83.3333 MHz clock and activated.

2.2.3 Gigabit transceiver Clock Domains

The external compensated Reference Oscillator is used as reference for the FPGA internal Phase Locked Loop (PLL) responsible for the 1.5 GHz serial data stream transmission and reception. The 75 MHz TX core clock is also generated from this reference clock. It controls the transport of the data between the FIFO blocks to the Optical Link module.

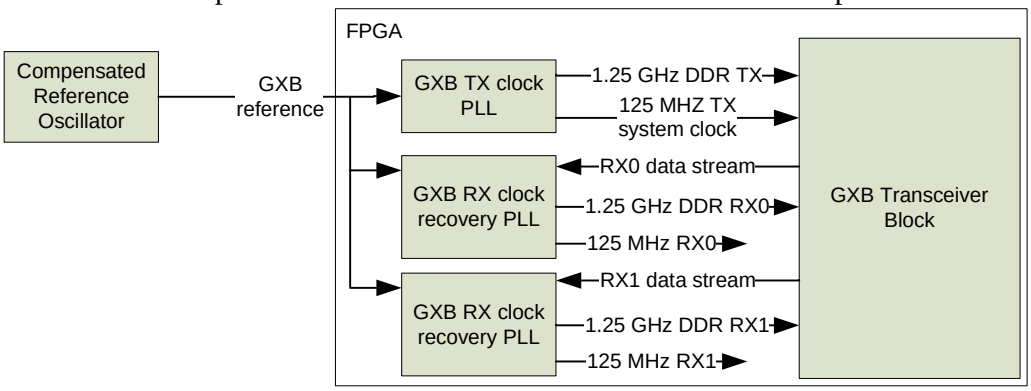

Figure 5: GXB RX0, RX1, TX Clock Domains

2.2.4 SHARC DSP memory port and transmitter clock domains

The base board of the SHARC DSP connector has a common system clock distribution; also the FOL FPGA is connected to this system clock of the baseboard. The FPGA internal PLL secures the stable operation of the DSP communication interfaces and compensates for phase offsets caused by transmission line length of the clock distribution network. The length compensated clock domain is used when signals to the SHARC DSP are driven by the FPGA, this includes acknowledge on lines on link port tree and four and the data and clock generation on link port one and two.

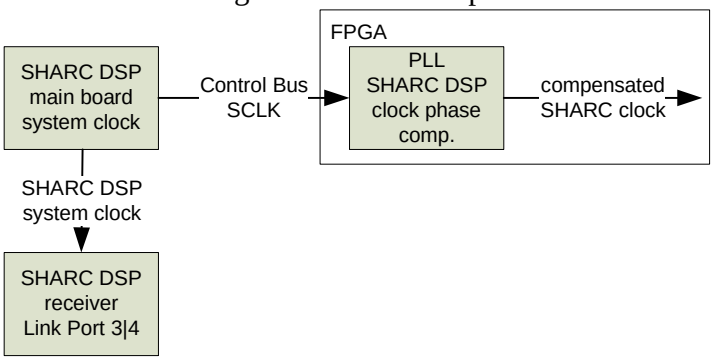

Figure 6: SHARC DSP System clock distribution

2.2.5 SHARC DSP link port receiver clock domain

The link ports three and four are used to receive data from DSP. Each transmitter link port of the connected DSP sends a LCLK signal that is used to clock in data to the FPGA internal link port receiver FIFO. The following graphic shows the DSP link ports clock domains of the link ports three and four that is used to clock in data from DSP.

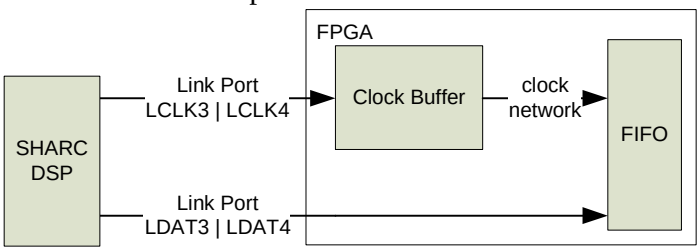

Figure 7: SHARC DSP link port receiver clock domain

2.3 FOL Transmitter data path

The transmitter uses a clock frequency of 750 MHz for the data stream generation of the serializer and deserializer modules (SERDES). Serial data is transmitted via a double data rate (DDR) output register within the transmitter module. The connected clock domains of the FOL transmitter path are shown in the following graphic.

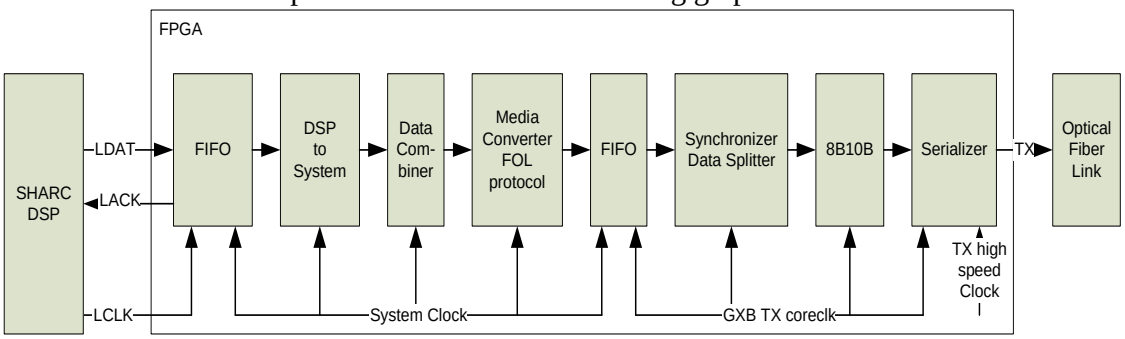

Figure 8: FOL transmitter data path

2.4 FOL Receiver data path

Received data from another FOL transmitter module is asynchronous to the transmitter clock domain of the local FOL. The two receiver modules operate with clocks asynchronous to the local transmitter module and synchronous to the external Fiber optical link input data stream. Therefore two PLLs are connected to the GXB reference clock input of the FPGA. The clock recovery is done by each of the two receiver PLLs that use the external reference clock oscillator as starting point of a frequency tuning process. When the recovered 1.5 GHz frequency is in the range of the transmitter frequency +-80 PPM (parts per million), the locking status of the receiver PLL is reached and the receiver serial data stream is sampled by the transmitter clock. The PLL is also used to generate the 75 MHz parallel receiver data clock signal that is used for 16 bit parallel data transport within the FPGA. The PLLs' low frequency output is synchronous to the transmitter frequency of the adjacent SHARC DSP baseboard module. This clock is used to clock in receiver data to a FIFO that decouples from the receiver clock domain. To avoid data overflow in that decoupling FIFO, only data words that are marked as non idle character are stored. A connected FSM controls the data decoding. The overview of the FOL receiver clock domains is shown in the following drawing:

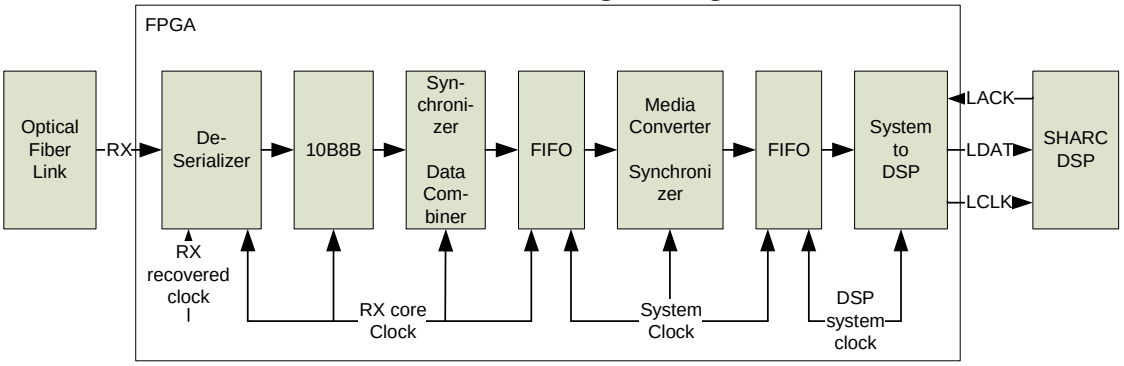

Figure 9: FOL receiver data path

3 System functionality

This section describes the Functions that are implemented within the FPGA.

3.1 Initial start up

This section describes the startup behavior of the FOL FPGA module.

- After activation of the power supply the configuration bit stream is transferred to the FPGA by the configuration device.
- After FPGA configuration the external reference oscillator is configured and enabled.
- The two receiver clock recovery PLLs get the external reference clock and try to lock to the incoming receiver data. The recovered clocks are used for data sampling and the parallel data transfer to the receiver FIFO.
- The reference oscillator clock activates the locking mechanism of the GXB transmitter PLL that receives the reference clock. After locking of the reference PLL the GXB transmitter module transmits serial data and control words that are coded as 8B10B. This leads to a serial transmitter data rate of 1.5 Gigabits/sec.
- After lock of the transmitter PLL the FOL sends continuously Idle and Synchronization words via the fiber link to the connected receiver FOL and the receiver FPGA starts to synchronize the receiver PLL.
- The received data is used for synchronization of the incoming 8B10B protocol and the 16 bit word synchronization.

3.1.1 Configuration of the external reference oscillator

The external 20 MHz oscillator has to be stable first. Then the connected PLL locks. As long as the PLL is not locked the configuration module is in reset status.
When locked it starts to readout the current configuration from the external reference oscillator. Depending on the internal settings the new configuration registers are written to reach an exact frequency of 83.3333 MHz. The configuration is then verified. When correct values are written the external reference oscillator is enabled. Then the FPGA internal GXB transceiver PLL gets the reference clock.

3.1.2 Calibration of the GXB transceiver modules

The external 20 MHz oscillator has to be stable first. Then the connected PLL locks. As long as the PLL is not locked the configuration module is in reset status.
When locked the reset is removed and the GXB calibration block starts to calibrate against production variances and thermal drifts.

3.1.3 GXB reference oscillator PLL

The GXB reference oscillator PLL is used to multiply the GXB reference clock by a factor of 0.9 and 9. The 75 MHz clock is used for the 16 Bit data and control word indicator transfer via the FOL transmitter and as general system clock. The serial data is transferred by the synchronous 750 MHz clock in double data rate with a 1.5 GHz data rate. The PLL lock status is used to hold all connected state machine in reset status when the generated system clock is not stable.

3.2 Transmitter Synchronization protocol

The GXB transmitter is configured in that way that 16 Bits data and 2 bits control data are transferred to the transmitter fiber link using 8B10B protocol.
The used idle word consists of two different idle characters. The first is used to synchronize to the eight bit boundary; the second is used to align to 16 bit boundary.

3.2.1 GXB receiver clock recovery

The receiver clock domain uses the reference oscillator clock and the input data bit stream for locking purpose. The clock recovery starts with the reference clock multiplies the input frequency by 0.9 and 9 and tries to reach the locking window with the reference clock. When reached, the tuning mechanism switches to the mode: Lock to data stream. When data stream is stable the PLL tries to lock to the input data stream. When reached, the PLL is locked and the receiver clock domains reset is removed. The reset is set again when the receiver is no longer synchronous with the PLL clock.

3.2.2 GXB receiver synchronization

By serializing the 8B10B data and the control indicator the bit order is lost when recovered. Therefore a synchronization word has to be transferred to restore the synchronization within the data stream. A special 8B10B character is used to indicate byte alignment. This also brings that most of 8B10B control words are no longer allowed to have a unique synchronization character. When the transmitter is idle it continuously sends the byte synchronization character that indicates no data (IDLE character) and synchronization bit order.

3.2.3 Receiver 8B10B synchronization

When the clock recovery PLL is locked the 8B10B receiver data is used to synchronize to the eight bit boundary. The data is shifted to the correct position and the synchronization status is set to stable data reception.

3.2.4 Receiver 16 bit word synchronization

When the eight bit boundary is synchronized the sixteen bit synchronizer starts to synchronize to the sixteen bit boundary. When 16 bit boundary character is read the 16 bit and control bit recovery is stable. As long as the 8B10B indicates no error and the PLL is in lock the Status indicates a stable link from transmitter to the receiver.

3.3 FOL Protocol

3.3.1 Standard transfer

Data from the DSP is transported via FIFO to the FOL TX clock domain. The DSP data consists of several 32 bit words. Therefore an additional 32 bit indicator character is used to indicate the 32 bit boundary. This 32 bit synchronization request is generated by the DSP data receiver module and is send before the first DSP data half word is transferred. The receiver marks the data with the 32 bit synchronization bit. This 32 bit synchronization is then used by the DSP data transmitter of the adjacent SHARC DSP module.

3.3.2 Error condition when no read out occurs

The FOL observes the status of the Fiber Link by observing the 8B10B parity status. A single bit error within the data character is securely found, Double bit errors within one 10 bit word is not surely detected.
When the receiving SHARC DSP does not read the data from the FOL the data transfer to the receiving FOL link module is stopped by disabling the acknowledge from the sending SHARC DSP.
The status of the DSP data transmitter FIFO in the receiving FOL link is observed. When the FIFO is half full the module will remove the acknowledge control signal from the sending DSP board. To achieve this, the fiber optical transmitter of the adjacent FOL module will send a stop sending character to the sending DSP module that removes the link acknowledge for the transmitter FOL.

3.4 SHARC DSP Memory Slave functionality

The memory mapped bus of the SHARC DSP is connected to the FOL module to access internal registers of the FOL FPGA implementation.

3.4.1 Memory Bus registers of previous installed Wiese Module

The previous installed modules in the SLS have the following configuration and status register bits: Only the 4 LSB bits are connected. The other bits have to be masked out.

Word Address Offset	Register Name	Bit	Content	Default
0x00	Configuration Register	0	0: selects Link Port 2 as data transmission Link Port, 1: selects Link1 as data transmission Link Port	0
0x00	Configuration Register bit	1	0: selects Link Port 4 as data receiver Link Port, 1: selects Link Port 3 as data receiver Link Port	0
0x00	Configuration Register bit	2	0: normal mode, 1: resets transmitter and receiver modules	0
0x00	Status Register bit	3	Ready for Data RFD status output of fiber link transmitter, only active when receiver module sends enable data, so receiver and transmitter sides are both locked. And data is synchronous on the link.	
0x02	Trigger Select Register bit	0	0: Trigger input B active, 1: Trigger input A active	0
0x02	Trigger Level Register bit	1	0: high active trigger input selection, 1: low active trigger input selection	0
0x02	Trigger enable Register bit	2	1: enables output IO to DSP IRQ2, 0: IRQ2 in mode high impedance	0
0x02	Low Clock Register bit	3	1: selects low clock on fiber links, 0: high speed clock selected	0

Table 2: WS9003 Configuration | Status registers

3.4.2 SHARC DSP memory mapped port

The new module is implemented as bus slave that allows access of status and control registers. Synchronous with the DSP system clock the memory slave data and acknowledge signal line is driven by the FPGA. This is shown in the following graphic:

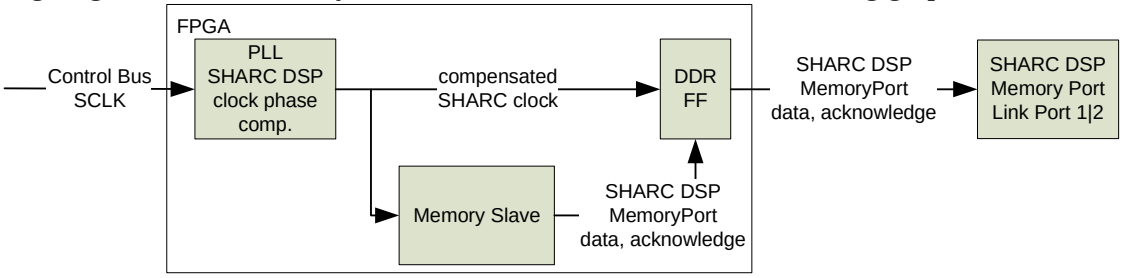

Figure 10: DSP to FPGA data transfer

3.4.3 Memory Bus Status Registers of new FOL module

The status register bits allow reading the release version and date of the installed firmware. The status of the Fiber connection is also available. The transmitter status bits indicate when the transmitter is initialized. The receiver status bits indicate a correct reception of the data from via fiber connected DSP module. Only the eight lower data on the memory port bits are connected. The other register bits should be masked out.

Word Address Offset	Register Name	Content	Data Type
0x00..0x07	Firmware ID	"FOLSHARC" (ASCII)	ASCII
0x08	Firmware Revision	0: Test, 1..255 release ID	unsigned char
0x09	Firmware Date	1..31	unsigned char
0x0A	Firmware Month	1..12	unsigned char
0x0B	Firmware Year	00..99	unsigned char
0x10	Transmitter 1 status	0 | 1 : transmitter (in)|active	LSB bit
0x11	Transmitter 2 status	0 | 1 : transmitter (in)|active	LSB bit
0x12	Receiver 1 status	0 | 1 : receiver data (in)|stable	LSB bit
0x13	Receiver 2 status	0 | 1 : receiver data (in)|stable	LSB bit
0x14	Receiver 1 error counter	0..255	unsigned char
0x15	Receiver 2 error counter	0.255	unsigned char

Table 3: Status Registers

3.4.4 Memory Bus Configuration Registers of new FOL module

These configuration registers can be used to configure the Trigger port behavior. IRQ2 is used to indicate a trigger to the connected DSP. In addition it can be used to reset and set parameters of the DSP link port connection including data transfer reset. Configuration Registers read back is possible.

Word Address Offset	Register Name	Content	Data Type	Default
0x20	Low speed selector for DSP Link Port 1	0: Half speed operation, 1: Full speed operation	LSB bit	0
0x21	Low speed selector for DSP Link Port 2	0: Half speed operation, 1: Full speed operation	LSB bit	0
0x22	Reset for FIFO DSP Link Port 1	0->1 transition resets data from transmitter FIFO of Link Port 1	LSB bit	0
0x23	Reset for FIFO DSP Link Port 2	0->1 transition resets data from transmitter FIFO of Link Port 2	LSB bit	0
0x24	Trigger select register	0: no Trigger to IRQ2, 1: Trigger A selected, 2: Trigger B selected, 3: Trigger C selected	2 LSB bits	0
0x25	Trigger polarity selector	0: Trigger input is high active, 1: Trigger is low active, default 0	LSB bit	0
0x26	Reset for FIFO DSP Link Port 3	0->1 transition resets data from transmitter FIFO of Link Port 3	LSB bit	0
0x27	Reset for FIFO DSP Link Port 4	0->1 transition resets data from transmitter FIFO of Link Port 4	LSB bit	0

Table 4: Configuration registers

3.5 SHARC DSP Link Ports

Four of the six DSP Link Ports of the connected SHARC DSP are connected to the FOL modules FPGA. Data transfer from DSP to FOL FPGA succeeds on Link Ports three and four. Data from link port three will be transferred to the left adjacent DSP FOL module via fiber line. Data from link port four is transferred to the right adjacent DSP module via fiber line. Data received from the left fiber is transferred to DSP link port one and data received from the right fiber is transferred to DSP link port two.
The transmitter DSP ports three and four of the DSP use an acknowledge signal that is used to stop data transmission when the signal ACK is driven inactive low. The acknowledge signal is driven low when the connected adjacent modules fiber is inactive, or when the adjacent module sends a stop transferring control word. The stop transferring control word is sent when the DSP transmitter FIFO is half full to prevent for lost data due to FIFO overflow on the receiver.

3.5.1 DSP Link Port data reception

The SHARC DSP configures the port three and four as transmitter. Data is transferred as nibbles (half byte). The DSP drives the link port clock signal LCLK and four data lines LDAT. Each data nibble is renewed with the rising edge of the LCLK signal. The FPGA reads the LDAT and transfers it to a receiver FIFO block that is then read by the internal transmitter system clock. Data is transmitted with the rising edge of LCLK by the SHARC DSP and read with the falling edge of LCK by the FPGA. Synchronous with the DSP system clock the LACK signal of the FOL receiver module is driven.

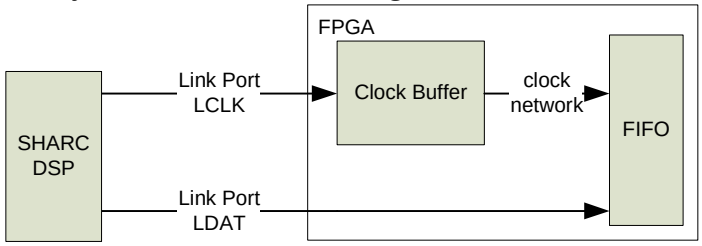

Figure 11: SHARC DSP link port LCLK and LDAT signal generation

3.5.2 FOL FPGA to SHARC DSP clock and data transmission

Synchronous with the DSP system clock the LCLK and LDAT signals of the FPGA to DSP transmitter module are driven. The following drawing shows the signal generation process:

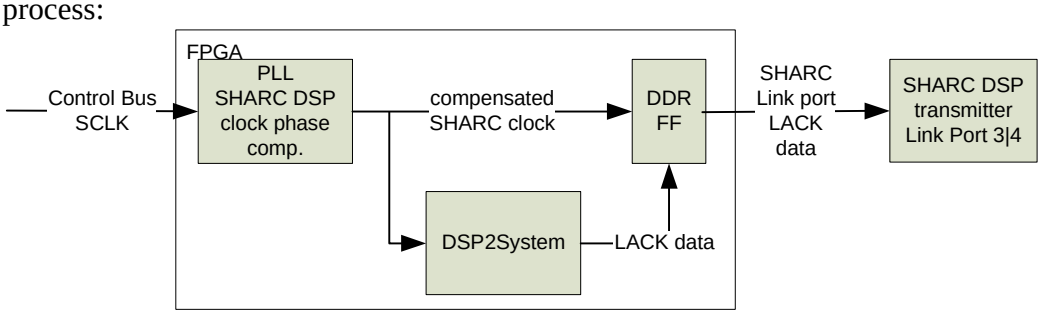

Figure 12: SHARC DSP link port LACK signal driver

3.5.3 DSP Link Port data transmission

The FPGA module System to DSP observes the LACK signal of the SHARC DSP. When the LACK signal is active high data stored in the connected FIFO is read by the module System to DSP and is transmitted via the LCLK and LDAT signal lines. Data is driven with the rising edge of LCLK and read with falling edge by the SHARC DSP.

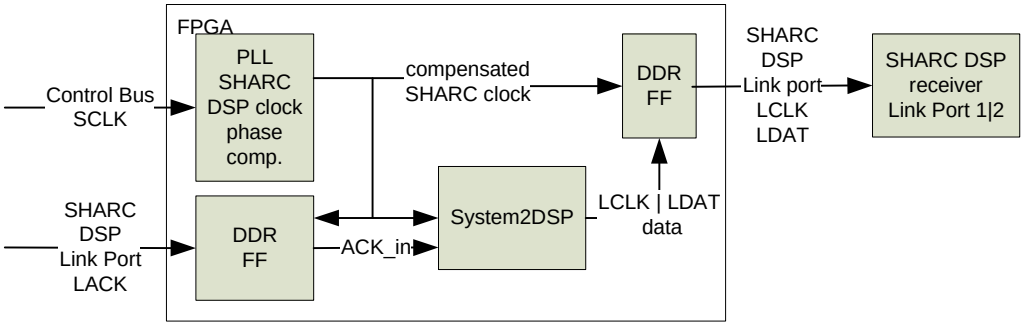

Figure 13: SHARC DSP link port LDAT, and LACK signal generation

3.6 SHARC DSP IRQ signal lines

Two IRQ signals are used to signal external trigger reception and error conditions to the connected SHARC DSP processor.

3.6.1 SHARC DSP IRQ1

The IRQ1 signal line is used to send an error condition event to the connected SHARC DSP. This happens when the status of the FIFO overflow observer has detected that data was lost or when the FOL is no longer stable. When an error occurs, the SHARC DSP will then signal an interlock status to the machine. Synchronous with the DSP system clock the IRQ1 signal line is pulsed after a new error condition event.

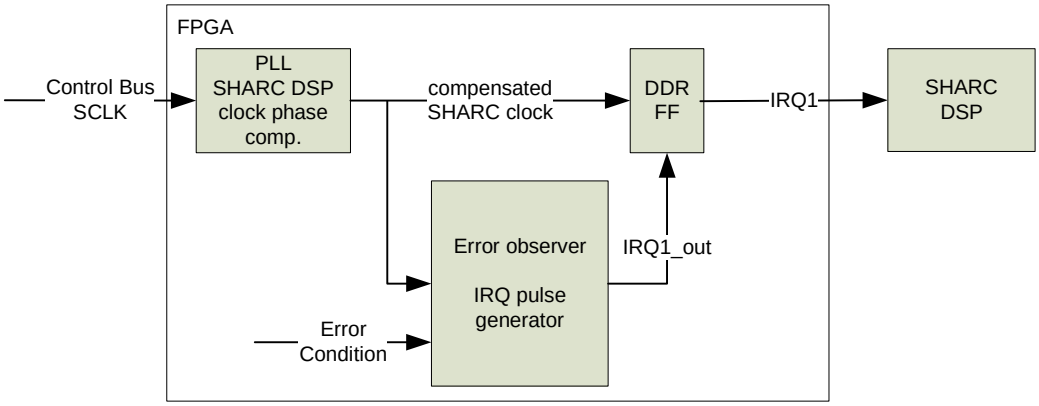

Figure 14: Error to IRQ1 signaling

3.6.2 SHARC DSP IRQ2

The FPGA has a configurable trigger configuration register that is configured via the SHARC DSP memory mapped port. It is used to select which trigger will be observed by the Trigger Observer module. The trigger polarity can also be selected. The default is no trigger is observed and trigger is active high. Depending on the trigger selection control register the trigger input A, B or C is observed. Synchronous with the DSP system clock the IRQ2 signal line is pulsed after a trigger event.

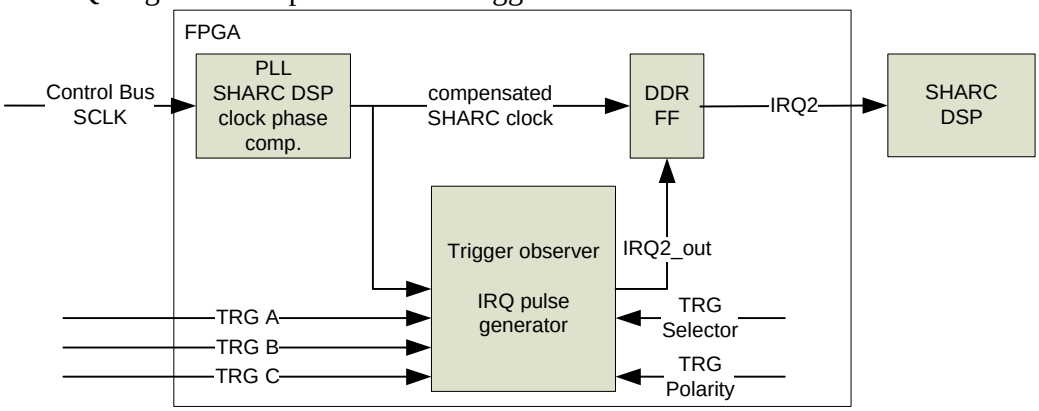

Figure 15: Trigger to IRQ2 signaling

4 Firmware and Board Simulation Interface

4.1 Simulation interface Test Bench

To simulate the behavior of the FOLSHARC board and communication protocols on the fiber optical link, as also to the DSP SHARC Processor memory interface, a test bench has been written. The Test Bench consists of several simulation modules that are listed up in this section.

4.1.1 Top Level Test Bench behavioral simulation

This is the simulation module of the Wiese SHARC DSP Base Board including the DSP processor. This module simulates the connection of the SHARC DSP with the Fiber Optical Link module. Additional Fiber Line connecting and removing is also simulated within this part of the test bench. It is possible to instantiate more than one FOL module here if needed.

4.1.2 ADSP 21060 behavioral simulation

This simulation module is used to stimulate data transfers by the DSP processor. It simulates the behavior of the analog devices SHARC DSP. The data transfer to and from the FOL is initiated from here. This module simulates also the memory mapped port from the SHARC DSP to the FOL and initiates the startup phase. Also the link port communication of the SHARC DSP is initiated here.

4.2 Fiber Optical Link Board Simulation Model

The simulation Test Bench of the FOL hardware contains some digital simulation models to simulate the data transfer on the FOL. The following table includes behavioral models that are used. Details can be found within the test benches of each module.

Module:	Description
FolSharcDIOV10_1	This is the Top Level of the FOL schematic simulation model. It describes how the schematic is combined of several schematic sheets.
SHARC IO Pack Connector	This is the simulation model of the SHARC IO Pack connector to the base board simulation model.
Level Converter	This is the simulation of the Level Converter schematic.
Optical Transceivers	This module includes the simulation of the optical transceiver modules.
Power Distribution	This module simulates the Power Distribution on the FOL board.
CYCLONE_IV_GX	This module includes the FPGA configuration and the IO pins of the Cyclone IV GX FPGA.
FOL SHARC PCB types	This package includes the description of the bus specification types.
EP4CGX15BF14C6 with firmware instance	Simulation model of the Cyclone IV GX FPGA: This simulation model instantiates the firmware and the simulation of the configuration of the FPGA.

Table 5: FOL simulation modules

4.3 Digital IC Simulation modules

The simulation Test Bench contains some digital simulation models to simulate the data transfer on the main board and the FOL. The following table includes behavioral models that are used. Details can be found within the test benches of each module.

Module:	Description
RESISTOR	Simulation model of a resistor
ZERO_RESISTOR	Simulation model of a 0 Ohm resistor
CAPACITOR	Simulation model of a capacitor
INDUCTOR	Simulation model of an inductor
FERRITE	Simulation model of a ferrite
JUMPER	Simulation model of a jumper
DIODE	Simulation model of a diode
LED	Simulation model of a LED
OSCILLATOR	Simulation model of an oscillator
XO_OSC_20	Simulation model of an 20 MHz oscillator
TXB0106PWR	Simulation model of device TXB0106PWR
AFBR_53D5EZ	Simulation model of device FBR_53D5EZ
CDCLVD1204RGTT	Simulation model of device DCLVD1204RGTT
SL_SI570BAC000304DG	Simulation model of device SL_SI570BAC000304DG
TI_TPS54620RGYT	Simulation model of device TI_TPS54620RGYT
LT1963AEST_3V3	Simulation model of device LT1963AEST
MAX_MAX16029TGP	Simulation model of device MAX16029TGP
NB100ELT23LDG	Simulation model of device NB100ELT23LDG
NCP566ST12T3G	Simulation model of device NCP566ST12T3G
JTAG_CONN	Simulation model of a JTAG_CONN
EPCS16SI8N	Simulation model of the device EPCS16SI8N

Table 6: Simulation library for digital representation of used ICs

Appendix

Figures

Tables