Addressing the QDRec V1x

Setting the VME Board Base Address

Using a VME 64x Crate, the board base address is set according to the slot geographical address Map. The VME Address switch SW4 should be disabled (all switch in position off) to assure a correct address decoding. Any 5 consecutive address line range can be used (A31..A27; A27..A22 etc…) for the board address mapping, giving a maximal address space of 128 Mbyte per VME Slot if using the 5 upper address lines (A31.. A27). In QDRec V11 is this range programmed into the FPGA and should be specified by the user. In QDRec V12 the range is selected by a 16 position rotative switch.

Using a non VME 64x crate, the VME board base address is set according to switch SW4, bit position 1 to 5. Switching to the „ON“ position, drives the comparator line to GND.

At this time the Board will only respond to A32/D32 addressing mode.

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

Example 1: SW4[7..0] == x | x | x | ON | OFF | OFF | OFF | ON means a Board Base Address of HEX 0x70000000 to 0x77000000

Geographic Address Map on a VME 64x Crate

Slot	VME - Slot Address using SW4	IOC VME – Address Map
0	F8xxxxxx-FFxxxxxx	Not Used
1	F0xxxxxx-F7xxxxxx	0400000-07FFFFF
2	E8xxxxxx-EFxxxxxx	0800000-0BFFFFF
3	E0xxxxxx-E7xxxxxx	0C00000-0CFFFFF
4	D8xxxxxx-DFxxxxxx	1000000-13FFFFF
5	D0xxxxxx-D7xxxxxx	1400000-17FFFFF
6	C8xxxxxx-CFxxxxxx	1800000-1BFFFFF
7	C0xxxxxx-C7xxxxxx	1C00000-1FFFFFF
8	B8xxxxxx-BFxxxxxx	2000000-23FFFFF
9	B0xxxxxx-B7xxxxxx	2400000-27FFFFF
10	A8xxxxxx-AFxxxxxx	2800000-2BFFFFF
11	A0xxxxxx-A7xxxxxx	2C00000-2FFFFFF
12	98xxxxxx-9Fxxxxxx	3000000-33FFFFF
13	90xxxxxx-97xxxxxx	3400000-37FFFFF
14	88xxxxxx-8Fxxxxxx	3800000-3BFFFFF
15	80xxxxxx-87xxxxxx	3C00000-3FFFFFF
16	78xxxxxx-7Fxxxxxx	4000000-43FFFFF
17	70xxxxxx-77xxxxxx	4400000-47FFFFF
18	68xxxxxx-6Fxxxxxx	4800000-4BFFFFF
19	60xxxxxx-67xxxxxx	4C00000-4FFFFFF
20	58xxxxxx-5Fxxxxxx	5000000-53FFFFF
21	50xxxxxx-57xxxxxx	5000000-53FFFFF

VME Offset Register Description

VME Offset	Bit	Description
0x0000	All	**Odd DDC FIFO access** When Bit0 of control register at 0x10 is set, reading or writing to this address accesses the fifo registers of DDC1(Lword) and DDC3(Hword)
0x0004	All	**Even DDC FIFO access** When Bit0 of control register at 0x10 is set, reading or writing to this address accesses the fifo registers of DDC2(Lword) and DDC4(Hword)
0x0008	All	**All DDC FIFO access** When Bit0 of control register at 0x10 is set, writing to this address accesses the fifo registers of DDC1(Lword) and DDC3(Hword), in parallel with DDC2(Lword) and DDC4(Hword). A reading at this address is only in D64 VME mode allowed.
0x000C	All	**FIFO Reset** Writing to this address resets all FIFO registers
0x0010	0	**VME access enable** 0 ➔ Disable FIFO VME access ; 1 ➔ Enable VME Access
	[2..1]	**Gated Acquisition** 00 ➔ Disable Acquisition 01 ➔ Enable Continous Acquisition 10 ➔ Disable Gated Acquisition 11 ➔ Enable Gated Acquisition
	[4..3]	**Acquisition Mode Select** 00 ➔ Fill FIFO, then stop acquisition while sending Data to DSP link port and Restart Acquisition when fifo empty. 01 ➔ When FIFO not empty then send directly FIFO Data to link port 10 ➔ Free run 11 ➔ Same as 00 using PAF FIFO depth
	5	**Link Port** 0 ➔ Enable Link Port 1 ➔ Disable Link Port
	[9..8]	**DDC Data format** 00 ➔ (default) Acquire only Magnitude Data 01 ➔ Acquire only Phase Data 10 ➔ not used 11 ➔ Acquire Magnitude and Phase Data
0x0020		**FIFO Status**
	0	Odd FIFO Empty Flag (EF)
	1	Odd FIFO Programmable Empty Flag (PAE)
	2	Odd FIFO Programmable Full Flag (PAF)
	3	Odd FIFO Full Flag (FF)
	4	Even FIFO Empty Flag (EF)
	5	Even FIFO Programmable Empty Flag (PAE)
	6	Even FIFO Programmable Full Flag (PAF)
	7	Even FIFO Full Flag (FF)
	8	Gate Monitor
	9	FiFo Busy Flag
0x0040		**Static Registers**
	0	DDC1 AGCNSEL
	[3..1]	DDC1 GAINADJ[2..0]
	4	n/c
	[7..5]	DDC1 SEL[2..0]
	8	DDC2 AGCNSEL
	[11..9]	DDC2 GAINADJ[2..0]
	12	n/c

	[15..13]	DDC2 SEL[2..0]
	16	DDC3 AGCNSEL
	[19..17]	DDC3 GAINADJ[2..0]
	20	n/c
0x0040	[23..21]	DDC3 SEL[2..0]
	24	DDC4 AGCNSEL
	[27..25]	DDC4 GAINADJ[2..0]
	28	n/c
	[31..29]	DDC4 SEL[2..0]
		FIFO Programmable Registers
0x0080	[31..0]	FIFO 1 & 3 PAE
0x0084	[31..0]	FIFO 1 & 3 PAF
0x0088	[31..0]	FIFO 2 & 4 PAE
0x008C	[31..0]	FIFO 2 & 4 PAF
		Carrier Offset Frequency
0x100	[31..0]	DDC1 COF Register Loading
0x104	[31..0]	DDC2 COF Register Loading
0x108	[31..0]	DDC3 COF Register Loading
0x10C	[31..0]	DDC4 COF Register Loading
0x10F	[31..0]	All DDC's COF Loading
		Sample Offset Frequency
0x200	[31..0]	DDC1 SOF Register Loading
0x204	[31..0]	DDC2 SOF Register Loading
0x208	[31..0]	DDC3 SOF Register Loading
0x20C	[31..0]	DDC4 SOF Register Loading
0x20F	[31..0]	All DDC's SOF Loading
		DDC Parameters
0x1000	[31..0]	DDC1
0x2000	[31..0]	DDC2
0x4000	[31..0]	DDC3
0x8000	[31..0]	DDC4
0xF000	[31..0]	All DDC's

QDRecV1x Address Map

Note : all addresses are to be considered as Offset Values to the Board Base Address

VME Offset	Byte 0	Byte 1	Byte 2	Byte 4	Comments
	MSB	**NMSB**	**NLSB**	**LSB**	
0x0	DDC3 MSB	DDC3 LSB	DDC1 MSB	DDC1 LSB	*FIFO Registers Read or Write*
0x4	DDC4 MSB	DDC4 LSB	DDC2 MSB	DDC2 LSB	*FIFO Registers Read or Write*
0x8	DDC3-4MSB	DDC3-4LSB	DDC1-2MSB	DDC1-2LSB	*FIFO Registers Write*
0xC	FIFO Reset				
0x10					*Board Status Read or Board Control Register Loading*
0x20			FIFO even	FIFO odd	*Fifo status register*
0x40	DDC4 static register	DDC3 static register	DDC2 static register	DDC1 static register	*Bit0: AGCNSEL; Bit[1..3]: GAINADJ[0..2]; Bit4: N/C Bit[5..7]: SEL[0..2]*
0x80					
0x100	DDC1 Carrier Offset Frequency Register Loading				*Preload DDC1 COF Register*
0x104	DDC2 Carrier Offset Frequency Register Loading				*Preload DDC2 COF Register*
0x108	DDC3 Carrier Offset Frequency Register Loading				*Preload DDC3 COF Register*
0x10C	DDC4 Carrier Offset Frequency Register Loading				*Preload DDC4 COF Register*
0x10F	DDC's Carrier Offset Frequency Register Loading				*Preload all DDC's COF Register*
0x200	DDC1 Sample Offset Frequency Register Loading				*Preload DDC1 SOF Register*
0x204	DDC2 Sample Offset Frequency Register Loading				*Preload DDC2 SOF Register*
0x208	DDC3 Sample Offset Frequency Register Loading				*Preload DDC4 SOF Register*
0x20C	DDC4 Sample Offset Frequency Register Loading				*Preload DDC0 SOF Register*
0x20F	DDC's Carrier Offset Frequency Register Loading				*Preload all DDC's SOF Register*
0x400					
0x404					
0x408					
0x40C					
0x1000-0x14FC	DDC1 Parameters				*DDC1 Word[0…255] Settings (1kByte space)*
0x2000-0x24FC	DDC2 Parameters				*DDC2 Word[0…255] Settings (1kByte space)*
0x4000-0x44FC	DDC3 Parameters				*DDC3 Word[0…255] Settings (1kByte space)*
0x8000-0x84FC	DDC4 Parameters				*DDC4 Word[0…255] Settings (1kByte space)*
0xF000-0xF4FC	all DDC's Parameters				*DDC's Word[0…255] Settings (1kByte space)*