Instruction Manual

Transition Board

TB 705

July 11, 2006 © Rev 1.3 R. Kramert

1 Manual Revision History

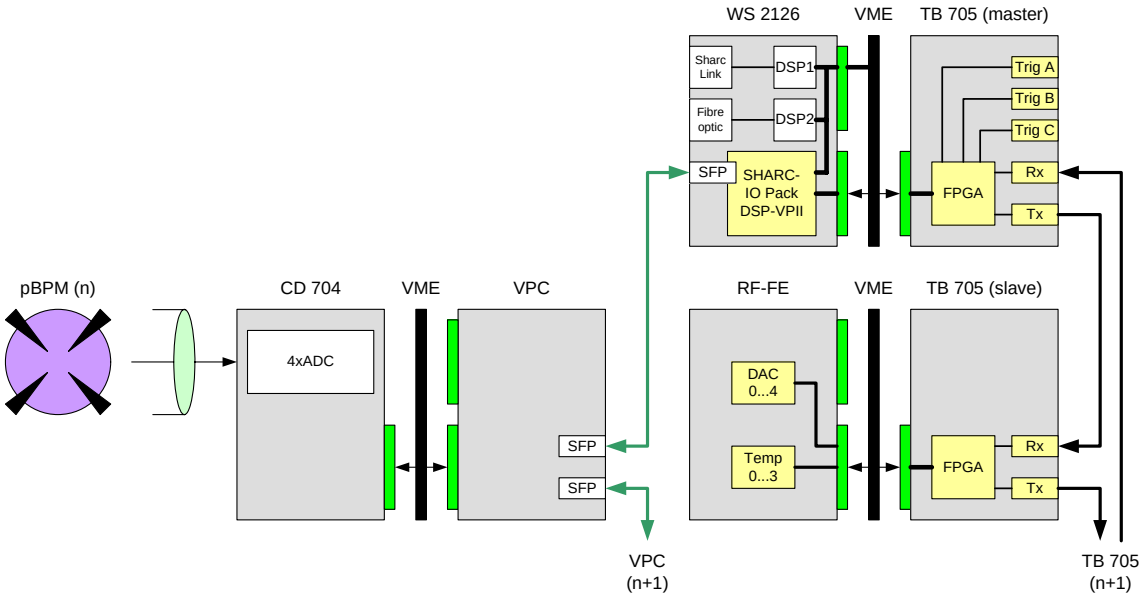
Version	Date	Name	Comments
A	Sept. 13, 2005	R. Kramert	TB-705A.doc
B	Oct. 18, 2005	R. Kramert	TB-705A 1.doc
C	Oct. 19, 2005	R. Kramert	TB-705A 1.2.doc
D	Jul. 11, 2006	R. Kramert, G. Marinkovic	TB-705 1.3.doc

2 Contents

3 Glossary

BPM	Beam Position Monitor
pBPM	photon Beam Position Monitor
RF-FE	Radio Frequency Front End
WS-2126	VME SHARC Cluster Module
TB-705	Transition Board

4 General Description



The TB-705 transition boards are part of the SLS-pBPM system. One TB-705 (referred as master) is communicating via VME/P2 rear connector with the WS-2126 DSP board and via RJ45 (serial link) to up to nine TB-705 (referred as slaves) boards. Three trigger lemo inputs are fed from the TB-705 master to the WS-2126 main board for synchronization purposes.
The TB-705 boards are daisy-chained via RJ45 running a serial link protocol. Each TB-705 (slave) board communicates to five gain DACs and four temperature sensors of the respective RF-FE via VME/P2 rear connector.

Please note: There is no difference in the TB-705 firmware or hardware concerning its use as master or slave board. The difference is a single bit provided by the "SHARC-IO Pack DSP-VPII" mezzanine board on the WS-2126 configuring the TB-705 to work as master or as slave (default).

The serial link between the TB-705s is CRC16 protected and addresses each TB-705 board individually to write or read data. The data to be written to the TB-705 slave (and hence to the RF-FE) has to be provided by the DSPs (WS-2126) by means of writing to a dual ported RAM buffer in the TB-705 master. The TB-705 master polls the data to be read by the DSP from each TB-705 slave and stores it in the buffer. This cyclic writing and reading of data to/from the TB-705 slaves is performed without any interaction needed by the DSPs.
The TB-705 master buffer consists of:

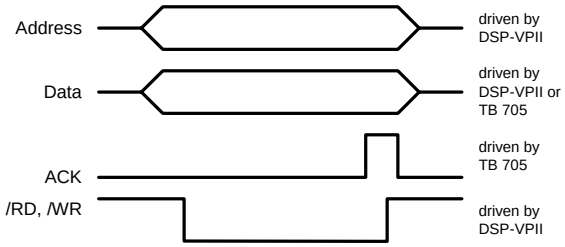
- the gain data, mapped to address 0x00…0x2C on memory page 0,
- the temperature data, mapped to address 0x00…0x23 on memory page 1,
- the free running counter, mapped to address 0x00 on memory page 4 and
- the link fault counter, mapped to address 0x01 on memory page 4.

Features TB-705:

- Gain data to 9 TB-705 slave boards controlling the individual 5 DACs on the RF-FE.
- Gain data is 16bit wide.
- Gain data is written to the DAC only if the gain values have changed in order to reduce noise due to the DAC clock.
- Temperature data from 9 TB-705 slave boards. Each TB-705 slave is controlling the individual 4 temperature sensors on the RF-FE
- Temperature is 16bit wide containing on bit 0 low temperature (< 10°C), on bit 1 high temperature (> 64°C), on bit 2 critical temperature (> 80°C), on bits 14-3 the temperature and on bit 15 the sign bit of the temperature.
- Free running counter with a resolution of 12.5ns.
- Serial link fault counter.

5 Timing Specifications

5.1 SHARC-IO Pack DSP-VPII to transition board TB-705:

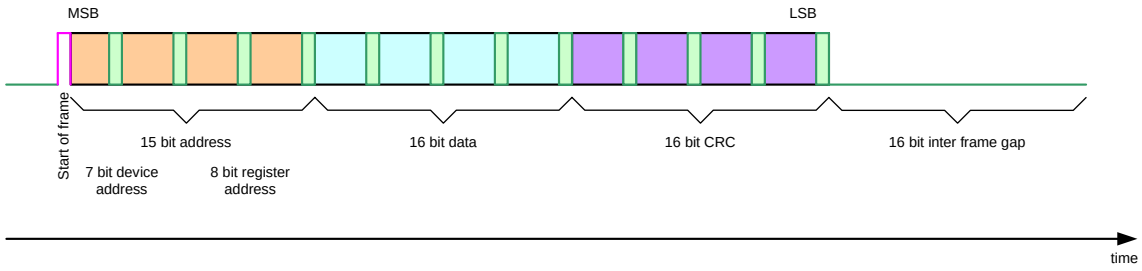


Address-decoding on the transition board TB 705 starts with a low level on /WR or /RD. The transition board logic asserts ACK high if:

- On write cycles, it has captured the data
- On read cycles, it has submitted stable data on the data bus.

It is necessary to deassert ACK as fast as possible after /RD or /WR are invalid. The logic waits for /RD and /WR inactive and terminates activity.

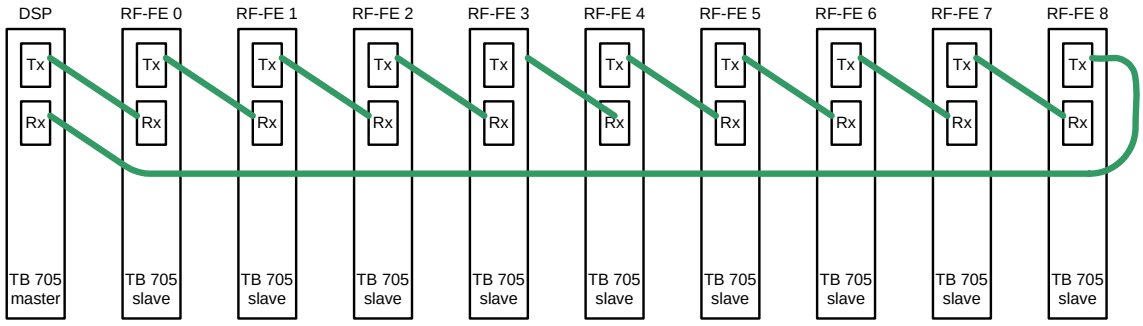
5.2 Serial Link:



The serial link transmits four 16 bit words. After each 4 bits of data a stuffing bit (inverted predeceasing bit) is inserted for resynchronization purposes. The frame starts with start of frame bit which is always “1”. Then the following 15bits form the address, indicating to which TB 705 and to which register the following 16 bit data is send. The frame is protected by a 16 bit crc checksum ($X^{15} + X^{14} + X^{10} + X^8 + X^7 + X^4 + X^3 + 1$). The frame finishes with an inter frame gap, violating the stuffing bit rule but allowing the receiver of such a link to detect cleanly the start of frame.

The TB-705 master keeps an error counter for lost frames and frames with an incorrect CRC checksum. This error counter can be read by the DSP at address 0x01 at page 4 in order to check for the link status and can be reset by writing any value to this error counter address.

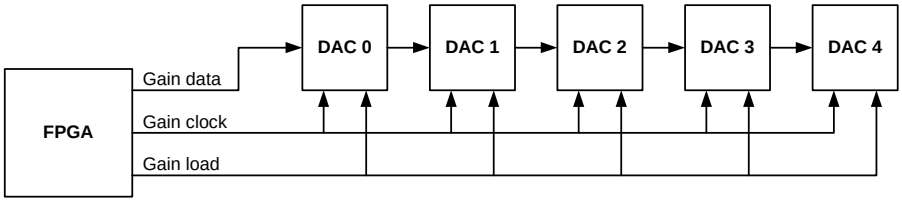
5.4 Daisy chain wiring of the serial link:



The TB-705 master board transmits with the MSB 7bits of the address word a device address to an appropriate TB-705 slave board. Because the boards do not know their own absolute address they simply assume every

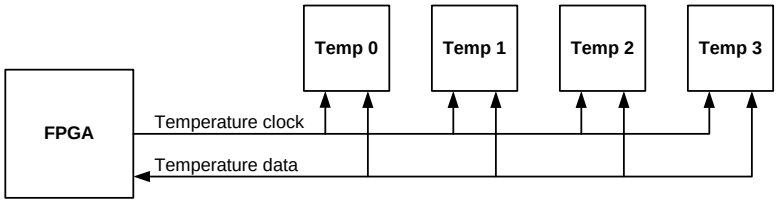
frame containing the address 0 to be their frame, all other frames are retransmitted by subtracting 1 from the 7bit device address.
The master receives for every frame transmitted a response, which is stored in the read buffer of the master. Hence giving the DSP an easy check whether data written to the TB-705 master buffer was transmitted successfully to the appropriate TB-705 slave. This implies that the data read from the TB-705 master is not automatically the data written to it but the response of a TB-705 slave. Therefore if the data written could be read back then this (gain) data was transmitted to the TB-705 slave and acknowledged.

5.3 Gain data setting:



Each RF-FE-module is equipped with fife 16bit gain setting DACs LTC1655 of Linear Technology. The gain data stream is started by the FPGA if new and changed gain data is received by the serial link. For more information concerning the DAC link please refer to the datasheet of the LTC1655 of Linear Technology.

5.3 Temperature data readout:



Each RF-FE-module is equipped with four temperature sensors LM-92 of National Semiconductors. The FPGA is accessing these temperature sensors by means of the I2C bus.
The temperature provided to the DSP is the value read from the LM-92 chip. This means it is 16bit wide containing:

- bit 0: low temperature flag (< 10°C),
- bit 1: high temperature flag (> 64°C),
- bit 2: critical temperature flag (> 80°C),
- bits 14-3: the temperature in 0.0625°C steps and
- bit 15: the sign bit of the temperature.

For more information concerning the temperature sensor link please refer to the datasheet of the LM-92 of National Semiconductors.

5.4 Free running counter:

The TB-705 master contains a free running counter at address 0x00 at page 4 needed for performance checks of DSP functions. This free running counter has a time resolution of 12.5ns and is 16bit wide, hence counting 0 to 12.5ns * (2^{16} -1) = 819187.5ns.

Please note: During the DSP access the free running counter register the free running counter itself is not stopped but a copy of the counter at the start of the reading is provided to the DSP as read value.

6 Address Map

Range 0x00...0x3F page 0:

Offset (Hex)	Bit [MSB:LSB]	Read/Write	Description
0x00	[15:0]	R/W	RF0, DAC0 RF-Gain
0x01	[15:0]	R/W	RF0, DAC1 RF-Gain
0x02	[15:0]	R/W	RF0, DAC2 RF-Gain
0x03	[15:0]	R/W	RF0, DAC3 RF-Gain
0x04	[15:0]	R/W	RF0, DAC4 RF-Gain
0x05	[15:0]	R/W	RF1, DAC0 RF-Gain
0x06	[15:0]	R/W	RF1, DAC1 RF-Gain
0x07	[15:0]	R/W	RF1, DAC2 RF-Gain
0x08	[15:0]	R/W	RF1, DAC3 RF-Gain
0x09	[15:0]	R/W	RF1, DAC4 RF-Gain
0x0A	[15:0]	R/W	RF2, DAC0 RF-Gain
0x0B	[15:0]	R/W	RF2, DAC1 RF-Gain
0x0C	[15:0]	R/W	RF2, DAC2 RF-Gain
0x0D	[15:0]	R/W	RF2, DAC3 RF-Gain
0x0E	[15:0]	R/W	RF2, DAC4 RF-Gain
0x0F	[15:0]	R/W	RF3, DAC0 RF-Gain
0x10	[15:0]	R/W	RF3, DAC1 RF-Gain
0x11	[15:0]	R/W	RF3, DAC2 RF-Gain
0x12	[15:0]	R/W	RF3, DAC3 RF-Gain
0x13	[15:0]	R/W	RF3, DAC4 RF-Gain
0x14	[15:0]	R/W	RF4, DAC0 RF-Gain
0x15	[15:0]	R/W	RF4, DAC1 RF-Gain
0x16	[15:0]	R/W	RF4, DAC2 RF-Gain
0x17	[15:0]	R/W	RF4, DAC3 RF-Gain
0x18	[15:0]	R/W	RF4, DAC4 RF-Gain
0x19	[15:0]	R/W	RF5, DAC0 RF-Gain
0x1A	[15:0]	R/W	RF5, DAC1 RF-Gain
0x1B	[15:0]	R/W	RF5, DAC2 RF-Gain
0x1C	[15:0]	R/W	RF5, DAC3 RF-Gain
0x1D	[15:0]	R/W	RF5, DAC4 RF-Gain
0x1E	[15:0]	R/W	RF6, DAC0 RF-Gain
0x1F	[15:0]	R/W	RF6, DAC1 RF-Gain
0x20	[15:0]	R/W	RF6, DAC2 RF-Gain
0x21	[15:0]	R/W	RF6, DAC3 RF-Gain
0x22	[15:0]	R/W	RF6, DAC4 RF-Gain
0x23	[15:0]	R/W	RF7, DAC0 RF-Gain
0x24	[15:0]	R/W	RF7, DAC1 RF-Gain
0x25	[15:0]	R/W	RF7, DAC2 RF-Gain
0x26	[15:0]	R/W	RF7, DAC3 RF-Gain
0x27	[15:0]	R/W	RF7, DAC4 RF-Gain
0x28	[15:0]	R/W	RF8, DAC0 RF-Gain
0x29	[15:0]	R/W	RF8, DAC1 RF-Gain
0x2A	[15:0]	R/W	RF8, DAC2 RF-Gain
0x2B	[15:0]	R/W	RF8, DAC3 RF-Gain
0x2C	[15:0]	R/W	RF8, DAC4 RF-Gain
0x2D...03F	[15:0]		Not used

Please note: The data read is not necessarily the data written but the data acknowledged by the corresponding TB-705 slave.

Range 0x00...0x3F page 1:

The temperature provided to the DSP is the value read from the LM-92 chip. This means it is 16bit wide containing:

- bit 0: low temperature flag (< 10°C),
- bit 1: high temperature flag (> 64°C),
- bit 2: critical temperature flag (> 80°C),
- bits 14-3: the temperature in 0.0625°C steps and
- bit 15: the sign bit of the temperature.

Offset (Hex)	Bit [MSB:LSB]	Read/Write	Description
0x00	[15:0]	R	RF(number of TB-705 slaves - 9), Temp Sensor 0
0x01	[15:0]	R	RF(number of TB-705 slaves - 9), Temp Sensor 1
0x02	[15:0]	R	RF(number of TB-705 slaves - 9), Temp Sensor 2
0x03	[15:0]	R	RF(number of TB-705 slaves - 9), Temp Sensor 3
0x04	[15:0]	R	RF(number of TB-705 slaves – 8), Temp Sensor 0
0x05	[15:0]	R	RF(number of TB-705 slaves – 8), Temp Sensor 1
0x06	[15:0]	R	RF(number of TB-705 slaves – 8), Temp Sensor 2
0x07	[15:0]	R	RF(number of TB-705 slaves – 8), Temp Sensor 3
0x08	[15:0]	R	RF(number of TB-705 slaves – 7), Temp Sensor 0
0x09	[15:0]	R	RF(number of TB-705 slaves – 7), Temp Sensor 1
0x0A	[15:0]	R	RF(number of TB-705 slaves – 7), Temp Sensor 2
0x0B	[15:0]	R	RF(number of TB-705 slaves – 7), Temp Sensor 3
0x0C	[15:0]	R	RF(number of TB-705 slaves – 6), Temp Sensor 0
0x0D	[15:0]	R	RF(number of TB-705 slaves – 6), Temp Sensor 1
0x0E	[15:0]	R	RF(number of TB-705 slaves – 6),Temp Sensor 2
0x0F	[15:0]	R	RF(number of TB-705 slaves – 6), Temp Sensor 3
0x10	[15:0]	R	RF(number of TB-705 slaves – 5), Temp Sensor 0
0x11	[15:0]	R	RF(number of TB-705 slaves – 5), Temp Sensor 1
0x12	[15:0]	R	RF(number of TB-705 slaves – 5), Temp Sensor 2
0x13	[15:0]	R	RF(number of TB-705 slaves – 5), Temp Sensor 3
0x14	[15:0]	R	RF(number of TB-705 slaves – 4), Temp Sensor 0
0x15	[15:0]	R	RF(number of TB-705 slaves – 4), Temp Sensor 1
0x16	[15:0]	R	RF(number of TB-705 slaves – 4), Temp Sensor 2
0x17	[15:0]	R	RF(number of TB-705 slaves – 4), Temp Sensor 3
0x18	[15:0]	R	RF(number of TB-705 slaves – 3), Temp Sensor 0
0x19	[15:0]	R	RF(number of TB-705 slaves – 3), Temp Sensor 1
0x1A	[15:0]	R	RF(number of TB-705 slaves – 3), Temp Sensor 2
0x1B	[15:0]	R	RF(number of TB-705 slaves – 3), Temp Sensor 3
0x1C	[15:0]	R	RF(number of TB-705 slaves – 2), Temp Sensor 0
0x1D	[15:0]	R	RF(number of TB-705 slaves – 2), Temp Sensor 1
0x1E	[15:0]	R	RF(number of TB-705 slaves – 2), Temp Sensor 2
0x1F	[15:0]	R	RF(number of TB-705 slaves – 2), Temp Sensor 3
0x20	[15:0]	R	RF(number of TB-705 slaves – 1), Temp Sensor 0
0x21	[15:0]	R	RF(number of TB-705 slaves – 1), Temp Sensor 1
0x22	[15:0]	R	RF(number of TB-705 slaves – 1), Temp Sensor 2
0x23	[15:0]	R	RF(number of TB-705 slaves – 1), Temp Sensor 3
0x24...03F	[15:0]		Not used

Please note: The data position has an offset depending on how many TB-705 slaves are in the daisy chain.

Range 0x00...0x3F page 4:

Offset (Hex)	Bit [MSB:LSB]	Read/Write	Description
0x00	[15:0]	R	Free running counter with a resolution of 12.5ns
0x01	[15:0]	R/W	Link error counter. Writing to this address resets the counter to 0.
0x02...03F	[15:0]		Not used

8 Connector Pin Specifications

8.1 Connector VME P2 Rear JR1:

IO-Level: 20A, 21A, 20C: open Collector, all others: 3.3Volt, 5V tolerant

Pin	Name	I/O	Definition
1A	TMP_CLK	O	I2C Temperature readout: Clock
2A	TMP_CSN		Not used
3A	TB-D0	I/O	Transition Board Data bus
4A	TB-D1	I/O	"
5A	TB-D2	I/O	"
6A	TB-D3	I/O	"
7A	TB-D4	I/O	"
8A	TB-D5	I/O	"
9A	TB-D6	I/O	"
10A	TB-D7	I/O	"
11A	TB-D8	I/O	"
12A	TB-D9	I/O	"
13A	TB-D10	I/O	"
14A	TB-D11	I/O	"
15A	TB-D12	I/O	"
16A	TB-D13	I/O	"
17A	TB-D14	I/O	"
18A	DSP_SCLK	I/O	Sharc-Bus Clock 40 MHz
19A			
20A	Gain_CLK	O	Gain Control: Clock
21A	Gain_LD	O	Gain Control: Load
22A	TB-D15		Transition Board Data bus
23A	Spare 2		Not used
24A			
25A			
26A			
27A			
28A			
29A			
30A			
31A	-12V_DC		Power

Pin	Name	I/O	Definition
1B	VCC_DC		+5 Volt Power
2B	GND		Power return
3B			
4B			
5B			
6B			
7B			
8B			
9B			
10B			
11B			
12B	GND		Power return
13B	VCC_DC		+5 Volt Power
14B			
15B			
16B			
17B			
18B			
19B			

20B			
21B			
22B	GND		Power return
23B			
24B			
25B			
26B			
27B			
28B			
29B			
30B			
31B	GND		Power return
32B	VCC_DC		+5 Volt Power

Pin	**Name**	**I/O**	**Definition**
1C	TMP_DATA	I/O	I2C Temperature readout: Data
2C	TMP S4		Not used
3C	TB-A0	I	Transition Board Address bus
4C	TB-A1	I	"
5C	TB-A2	I	"
6C	TB-A3	I	"
7C	TB-A4	I	"
8C	TB-A5	I	"
9C	TB-A6	I	"
10C	TB-A7	I	"
11C	TB-A8	I	"
12C	TB-RDn	I	Read Strobe
13C	TB-WRn	I	Write Strobe
14C	TB-ACK	O	Acknowledge
15C	TB-TRIG A	I/O	TB-Trigger Bus A for Sharc I/O-Pack
16C	TB-TRIG B	I/O	TB-Trigger Bus B for Sharc I/O-Pack
17C	TB-TRIG C	I/O	TB-Trigger Bus C for Sharc I/O-Pack
18C			
19C			
20C	Gain_DATA	O	Gain Control: Data
21C			
22C	TB-A9		Transition Board Address bus
23C	Spare 4	I	Not used
24C			
25C			
26C			
27C			
28C			
29C			
30C			
31C	+12V_DC		Power

8.2 Connector Serial Link TX RJ45 JP5:

Pin-Nr.	Signal	I/O	IO-Level	Description
1	Not used	O	RS-422	
2	Not used	O	RS-422	
3	TX_DATA	O	RS-422	Link data
4	*TX_DATA	O	RS-422	*Link data
5	Not used	O	RS-422	
6	Not used	O	RS-422	
7	nc			
8	nc			
9	GND			Ground
10	GND			Ground

8.3 Connector Serial Link RX RJ45 JP6:

Pin-Nr.	Signal	I/O	IO-Level	Description
1	Not used	I	RS-422,100 Ω	
2	Not used	I	RS-422,100 Ω	
3	RX_DATA	I	RS-422,100 Ω	Link data
4	*RX_DATA	I	RS-422,100 Ω	*Link data
5	Not used	I	RS-422,100 Ω	
6	Not used	I	RS-422,100 Ω	
7	nc			
8	nc			
9	GND			Ground
10	GND			Ground

8.4 Connector TX RJ45 JP7:

Pin-Nr.	Signal	I/O	IO-Level	Description
1	Not used	O	RS-422	
2	Not used	O	RS-422	
3	Not used	O	RS-422	
4	Not used	O	RS-422	
5	Not used	O	RS-422	
6	Not used	O	RS-422	
7	nc			
8	nc			
9	GND			Ground
10	GND			Ground

8.5 Connector RX RJ45 JP8:

Pin-Nr.	Signal	I/O	IO-Level	Description
1	Not used	I	RS-422,100 Ω	
2	Not used	I	RS-422,100 Ω	
3	Not used	I	RS-422,100 Ω	
4	Not used	I	RS-422,100 Ω	
5	Not used	I	RS-422,100 Ω	
6	Not used	I	RS-422,100 Ω	
7	nc			
8	nc			
9	GND			Ground
10	GND			Ground

8.6 Connector LEMO J3, 4, 5:

Connector	Signal	I/O	Level OUT	Level IN	Description
J3	TRIG A	I/O	3.3V	3.3V, 5V tolerant	Trigger IO
J4	TRIG B	I/O	3.3V	3.3V, 5V tolerant	Trigger IO
J5	TRIG C	I/O	3.3V	3.3V, 5V tolerant	Trigger IO

9 Jumpers

Jumper	Signal	Description
JP3	*Program	Initializes FPGA
JP4	*INIT	delays FPGA boot sequence

10 LEDs

LED	Description	
LED1 green	off: blinking:	TB-705 link not active TB-705 slave and link active
LED1 red	off: blinking:	TB-705 link not active TB-705 master and link active

11 Power Requirements

Approx. 0.2A at +5V

12 TB-705 Layout