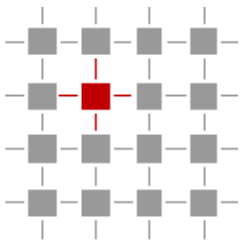
WS9002
SHARC IO-Pack

Differential
Link Channel
Receiver/Transmitter

WIESE
signal
verarbeitung



1 Manual Revision History

Version	Date	Name	Comments
0.0	25.04.98	jw	First edition
1.0	30.04.98	jw	released

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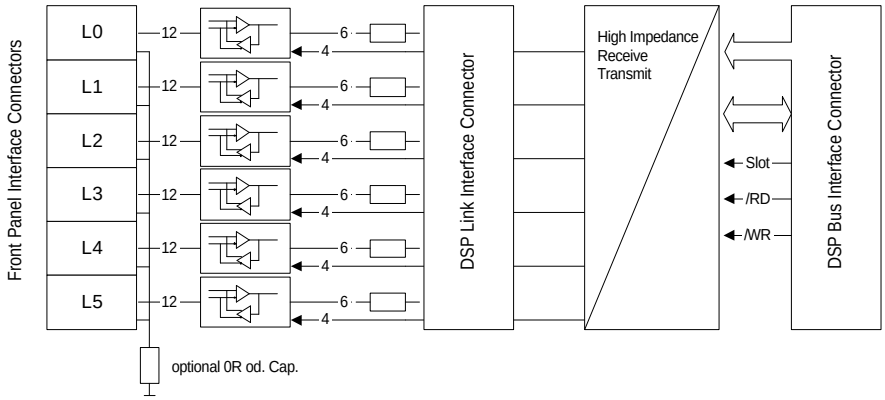
2 Contents

3 Glossary

- SHARC - The ***S***uper ***H***arvard ***AR***chitecture ***C***omputer is a high performance 32 bit IEEE floating point digital signal processor. AD21062 and AD21060 are two members of the SHARC family. The DSPs work at maximum frequency of 40 MHz. All instructions are execute within one cycle. The AD21062 contains 2 Mbits SRAM of internal dual ported memory whereas the memory size is 4 Mbit in case of the AD21060. Six link ports for I/O - or interprocessor communication at a data rate of 40 MByte each are provided. Refer to the ADSP-2106x SHARC User's Manual[1] for more details.

- Host access - The access with the highest priority to the SHARC DSPs is the host access. All interprocessor communication on the DSP bus stops if a host requests control of it. The VME or PCI bus master access to the SHARC DSPs acts as host access. Refer to the ADSP-2106x SHARC User's Manual for more details.

4 Blockdiagram



5 General Description

The WS9002 is a Size1 differential halfduplex Link Transceiver SHARC IO-Pack featuring:

- direction programmable at link base
- readable configuration register (no shadow required)
- physical link to connector interface for real point to point connections
- works up to 40 MByte/sec
- long line transmission

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6 SHARC IO-Pack Interface

6.1 DSP Bus Interface

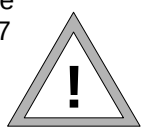
The SHARC DSP is a 32 bit machine so that the smallest addressable unit on the DSP bus is a 32 bit location. For addressing the SHARC IO-Packs only the lowest 8 address lines in junction with a piggy back select line for each DSP slot are used. For information about the address map on the DSP bus please refer to the manual of the motherboard.

6.1.1 DSP Bus Address Map

Address (Hex)	Read/Write	Description
#00	r/w	Control register

6.1.2 Register Contents

Note 1: Due to the fact that the DSP´s data width is 48 bit, only the higher 32 bit correspond to the 32 bit of the host bus side. DSP data bit 16 corresponds to host data bit 0, DSP data bit 47 corresponds to host data bit 31. The notation in this manual is from host side point of view.



Note 2: The contents of the Control Register is cleared within the power on reset.

6.1.3 Control Register

Offset address : $ 00 (read/write)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
not used				Link 5		Link 4		Link 3		Link 2		Link 1		Link 0	

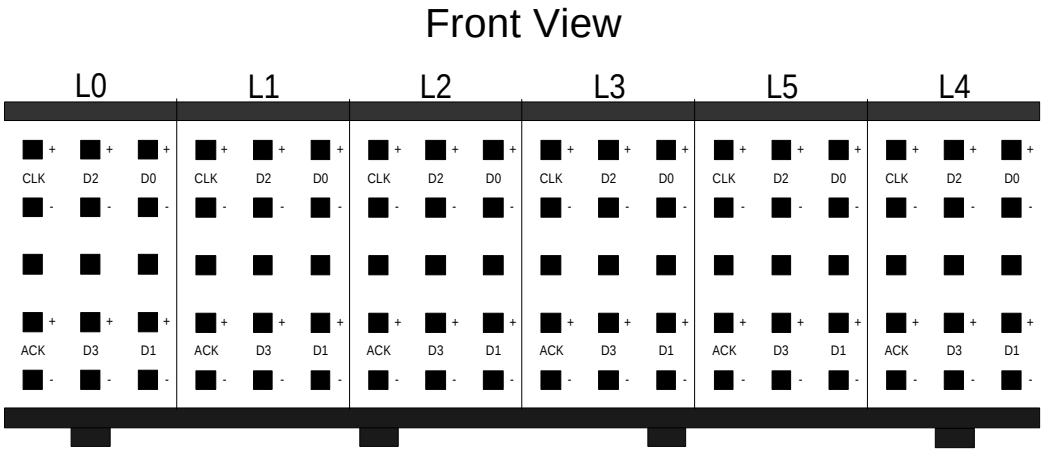
A write to this register will change the link configuration; a read on this register will return with the actual link configuration. The not used Bits will hold to ground on a read.

Function Table of the Control Register

MSB	LSB	Function per Link
0	0	High Impedance
0	1	Receive Data
1	0	Transmit Data
1	1	High Impedance

6.2 Front End Interface

The connector system used for the WS 9002 is a modified 2mm Z-Pack system.
Each channel needs 6 mm space in brightness, so the total amount for all Link channel is 36 mm. Exactly the IO-Pack dimension.
Each Link channel use 12 differential plus 3 shield pins. Each differential pair has it's own cable shield and all shields can pulled down via jumper at the source or destination side.



7 Getting Started

7.1 Hardware Configuration

Turn off power on the motherboard and remove it from it's slot. In case of a VME motherboard (e.g. WS21xx) it may be necessary to remove also the front panel.
Verify that the connectors on the motherboard and on WS9002 are free of dust and other objects that may cause loose contacts and insert the piggy back while keeping it parallel to the motherboard. Do not twist either the motherboard or WS9002 during installation.

7.2 Software Configuration

Depending on the contents of the configuration registers several working conditions of WS9002 are adjustable by software. These modes are discussed below.

7.3 Error Conditions

TBD

7.4 Example: WS 9002 Setup Sequence

First step: Power On Reset of WS 9002

Second step: Initialize the SHARC Links
Setup buffer, direction, clock and disable (tri-state) the SHARC pins

Third step: Configure WS 9002 via Control Register
Write your needed Link direction setup to the Control Register

Fourth step: Enable the SHARC Links

Fifth step: Start transmission
Use Core or DMA read/writes to transmit data over the link

Cycle : in your setup

8 Board Resources

none

9 SHARC IO-Packs

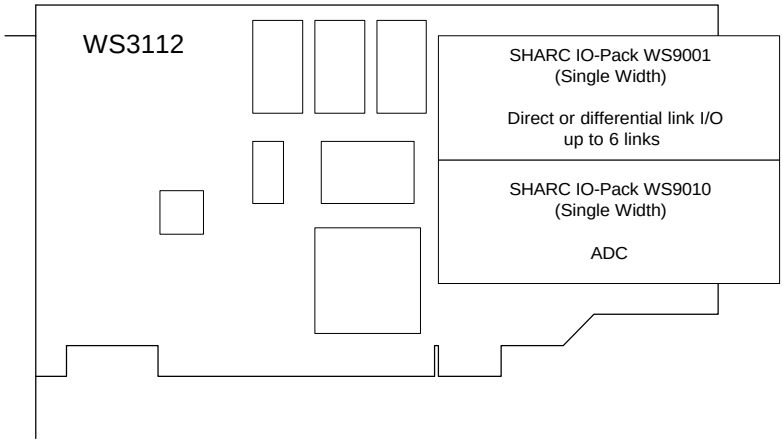
9.1 General Concept

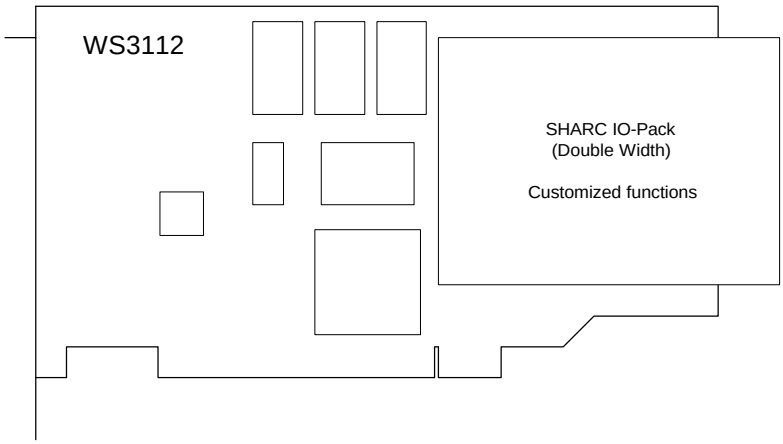
In general the link ports of the DSPs support fast communication between the DSPs and external data sources/sinks up to 40 Mbyte/s for each link *). To keep all options of communication paths, all 6 links of all 6 DSPs are routed to the SHARC IO-Pack front end connector.
A link bus with three links is routed to each DSP by bus jumpers. This allows DSP intercommunication without offboard hardware connections.
A very flexible I/O concept has been realized by introducing the SHARC IO-Packs. Each SHARC DSP now may "carry" a dedicated I/O interface. The range of I/O options may vary from simple link interconnections up to ADCs/DACs I/Os and fiber optic link interfaces.
In customized applications a SHARC IO-Pack also can cover more than one slot.
Depending on the kind of SHARC IO-Pack the SHARC signals which are routed to the front connectors may vary. Please refer to the specification of the SHARC IO-Pack which is in use.

*) The maximum speed is documented in the latest ADSP-2106x data sheet from Analog Devices.

9.1.1 SHARC IO-Packs On WS3112

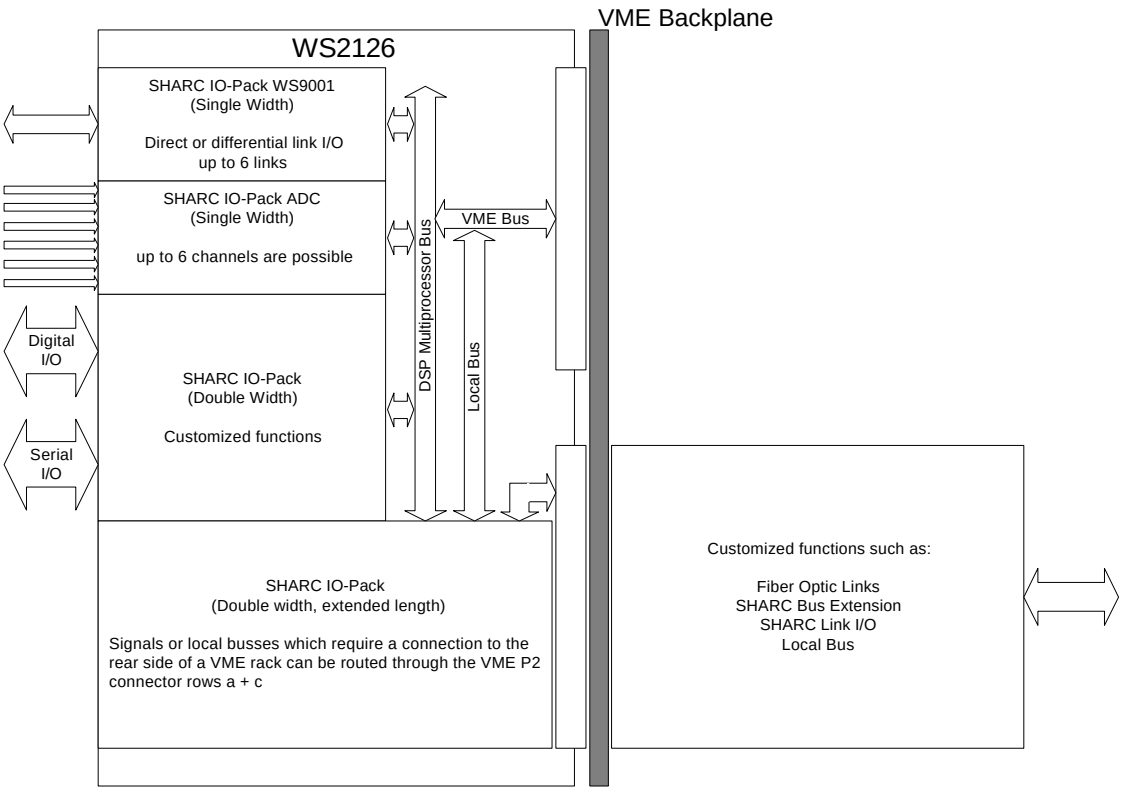
The pictures below pick up a few I/O options to give you an idea how to use SHARC IO-Packs on the PCI master/slave WS3112.





9.1.2 SHARC IO-Packs On WS2126

The picture below picks up a few I/O options to give you an idea how to use SHARC IO-Packs on the VME master/slave WS2126.
Due to the fact that the DSP bus connectors, the local bus connector and the P2 extension connector can be used by a SHARC IO-Pack configuration, the number of I/O alternatives is numerous.



9.2 SHARC IO-Pack Interface

All SHARC IO-Packs are memory mapped into the host address space and into the DSP external address area. For VME/PCI address info please refer to the manual of the motherboard in use.
The SHARC IO-Pack connectors (Molex) are designed for functional extensions of the DSP board. All important signals (from each SHARC) are routed to two corresponding connectors **XTn** and **XBn** ('**n**' is the SHARC processor number).
The user has access to all SHARC I/O resources: **LINK** ports, **SPORT** channels, **IRQ1** and **IRQ2**, **FLAG2**, **FLAG3**, and to most signals of the parallel local SHARC bus. Please refer to the detailed connector-description in the appropriate motherboard manual.
32 bit of the data bus (**SD16** ... **SD47**), 8 address lines (**SA0** ... **SA7**) and a select signal for the appropriate slot are routed to each SHARC IO-Pack.. The signal **/PIGGY_CS** is generated by the glue logic on the motherboard.
With the use of the signals **/RD** and **/WR** it is possible to interface devices to the SHARC bus and to generate waitstates if necessary. The lines **/DMARx** and **/DMAGx** interface hardware-controlled DMA channels.
There are some multipurpose lines: three trigger lines **TRGA ... TRGC.** They are all bus lines, connected to the SHARC IO-Pack connectors.

For more detailed description of the SHARC IO-Pack interface please refer to:

[3] SHARC IO-Pack Interface
Hardware Manual
Wiese Signalverarbeitung GmbH

and

ADSP-2106x SHARC User's Manual
Analog Devices

10 Connectors & Switches

10.1 SHARC IO-Pack Motherboard Connectors

Pin-Nr.	Signal	Description (Front)
1	FLAG3	SHARC Flag 3 Pin
2	TRGC	Trigger Bus C for SHARC I/O-Pack
3	FLAG2	SHARC Flag 2 Pin
4	DGND	Reserved for future use
5	TIMEXP	Timer expired
6	/IRQ1	Interrupt Request Line 1
7	/IRQ2	Interrupt Request Line 2
8	DT1	Data Transmit (SPORT 1)
9	/RST	Board Hardware Reset
10	TCLK1	Transmit Clock (SPORT 1)
11	TFS1	Transmit Frame Sync (SPORT 1)
12	DR1	Data Receive (SPORT 1)
13	RCLK1	Receive Clock (SPORT 1)
14	RFS1	Receive Frame Sync (SPORT 1)
15	DGND	
16	L5ACK	Link Port 5 Acknowledge
17	L5CLK	Link Port 5 Clock
18	L5D0	Link Port 5 Data D0
19	L5D1	Link Port 5 Data D1
20	L5D2	Link Port 5 Data D2
21	L5D3	Link Port 5 Data D3
22	+5VD	
23	DGND	
24	+5VD	
25	L4ACK	Link Port 4 Acknowledge
26	L4CLK	Link Port 4 Clock
27	L4D0	Link Port 4 Data D0
28	L4D1	Link Port 4 Data D1
29	L4D2	Link Port 4 Data D2
30	L4D3	Link Port 4 Data D3
31	DGND	
32	L3ACK	Link Port 3 Acknowledge
33	L3CLK	Link Port 3 Clock
34	L3D0	Link Port 3 Data D0
35	L3D1	Link Port 3 Data D1
36	L3D2	Link Port 3 Data D2
37	L3D3	Link Port 3 Data D3
38	+5VD	
39	n.c.	
40	L2ACK	Link Port 2 Acknowledge
41	L2CLK	Link Port 2 Clock
42	L2D0	Link Port 2 Data D0
43	L2D1	Link Port 2 Data D1
44	L2D2	Link Port 2 Data D2
45	L2D3	Link Port 2 Data D3
46	+5VD	
47	DGND	
48	DGND	
49	L1ACK	Link Port 1 Acknowledge
50	L1CLK	Link Port 1 Clock
51	L1D0	Link Port 1 Data D0
52	L1D1	Link Port 1 Data D1
53	L1D2	Link Port 1 Data D2
54	L1D3	Link Port 1 Data D3
55	+5VD	
56	L0ACK	Link Port 0 Acknowledge
57	L0CLK	Link Port 0 Clock
58	L0D0	Link Port 0 Data D0
59	L0D1	Link Port 0 Data D1
60	L0D2	Link Port 0 Data D2
61	L0D3	Link Port 0 Data D3
62	DGND	
63	TRGB	Trigger Bus B for SHARC I/O-Pack
64	TRGA	Trigger Bus A for SHARC I/O-Pack

Pin-Nr.	Signal	Description (Rear)
1	SA0	SHARC address bus (HOST: A2)
2	SA3	SHARC address bus (HOST: A5)
3	SA1	SHARC address bus (HOST: A3)
4	SA4	SHARC address bus (HOST: A6)
5	SA2	SHARC address bus (HOST: A4)
6	SA5	SHARC address bus (HOST: A7)
7	-12V	
8	+5VD	
9	DGND	
10	DGND	
11	/DMAR1	DMA Request 1 (Channel 7)
12	/DMAR2	DMA Request 2 (Channel 8)
13	DGND	
14	ACK	Memory Acknowledge
15	SD17	SHARC data bus (VME: D1)
16	SD32	SHARC data bus (VME: D16)
17	SD16	SHARC data bus (VME: D0)
18	DGND	
19	+12V	
20	BUS6	Bus Line
21	DT0	Data Transmit (SPORT 0)
22	/PIGGY_CS	SHARC I/O-Pack Chipselect
23	TFS0	Transmit Frame Sync (SPORT 0)
24	TCLK0	Transmit Clock (SPORT 0)
25	RCLK0	Receive Clock (SPORT 0)
26	DR0	Data Receive (SPORT 0)
27	BUS7	Bus Line
28	RFS0	Receive Frame Sync (SPORT 0)
29	+5VD	
30	SD18	SHARC data bus (VME: D2)
31	/RD	Memory Read Strobe
32	n.c.	
33	SD39	SHARC data bus (VME: D23)
34	/WR	Memory Write Strobe
35	SD37	SHARC data bus (VME: D21)
36	SD38	SHARC data bus (VME: D22)
37	SD35	SHARC data bus (VME: D19)
38	SD36	SHARC data bus (VME: D20)
39	SD34	SHARC data bus (VME: D18)
40	SCLK	System Clock (40 MHz)
41	SD33	SHARC data bus (VME: D17)
42	/DMAG2	DMA Grant 2 (Channel 8)
43	SD20	SHARC data bus (VME: D4)
44	/DMAG1	DMA Grant 1 (Channel 7)
45	SD30	SHARC data bus (VME: D14)
46	SD31	SHARC data bus (VME: D15)
47	SD28	SHARC data bus (VME: D12)
48	SD29	SHARC data bus (VME: D13)
49	SD26	SHARC data bus (VME: D10)
50	SD27	SHARC data bus (VME: D11)
51	SD24	SHARC data bus (VME: D8)
52	SD25	SHARC data bus (VME: D9)
53	SD47	SHARC data bus (VME: D31)
54	SD23	SHARC data bus (VME: D7)
55	SD22	SHARC data bus (VME: D6)
56	SD46	SHARC data bus (VME: D30)
57	SD21	SHARC data bus (VME: D5)
58	SD45	SHARC data bus (VME: D29)
59	SD19	SHARC data bus (VME: D3)
60	SD44	SHARC data bus (VME: D28)
61	SD42	SHARC data bus (VME: D26)
62	SD43	SHARC data bus (VME: D27)
63	SD41	SHARC data bus (VME: D25)
64	SD40	SHARC data bus (VME: D24)

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11 Technical Data

11.1 Power Requirements

TBD

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12 Trouble Shooting / Support

Voltages - Are all voltages within it´s specified limits ?

DSP host packing mode - If the access to the DSP(s) returns unexpected results, verify that the DSP works in the correct "host packing mode".

DSP bus priority - In most cases the DSPs work in a "hierarchical bus priority". Every time the DSP with the highest priority requests for the bus, all other DSPs are forced to stop their own bus activity. In some cases a "rotating priority" scheme is more suitable. The bus priority scheme can be modified by software (Control Register) or by hardware (DIP switch).

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List Of Literature

[1] ADSP-2106x SHARC User´s Manual, Analog Devices.
For newest Information and SHARC-FAQs look at: http://www.analog.com

[3] SHARC IO-Pack Interface Hardware Manual, Wiese Signalverarbeitung GmbH

Annex

ADC - AD9241 data sheet for detailed programming-/hardware Information
MUX - ADG406 data sheet for detailed programming-/hardware Information