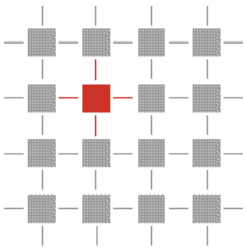
WS 9003

Fiber Optic Link SHARC IO-Pack

WIESE
signal
verarbeitung



1. Manual Revision History

Version	Date	Name	Comments
1.0	19.10.99	te	First edition
1.1	13.07.00	te	Register description updated

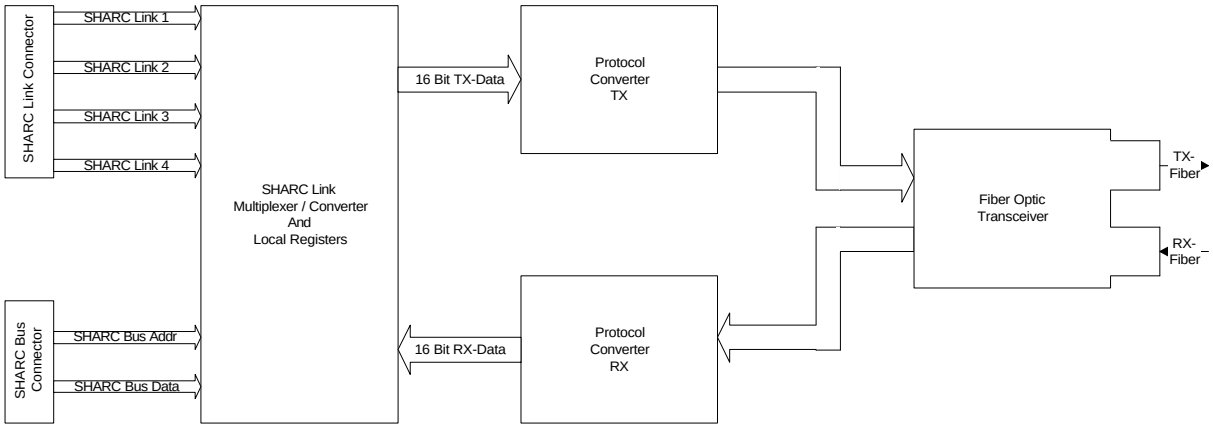
2. Contents

4. Overview

WS9003 Fiber Optic Link is a SHARC IO-Pack Interface which is able to transfer data over a fiber optic cable. You can select either SHARC link 1 or 2 as the transmitter link and SHARC link 3 or 4 as the receiver link.

5. Blockdiagram

WS9003 Fiber Optic Link
SHARC IO-Pack



6. Installation

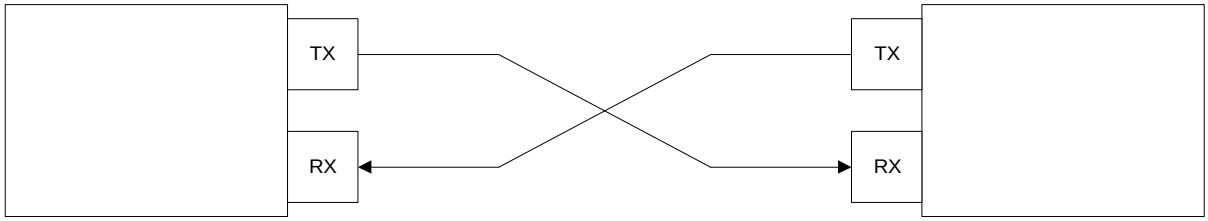
6.1 Hardware Configuration

Turn off power on the motherboard and remove it from it´s slot. In case of a VME motherbord (e.g. WS21xx) it may be necessary to remove also the front panel.
Verify that the connectors on the motherboard and on WS9003 are free of dust and other objects that may cause loose contacts and insert the piggy back while keeping it parallel to the motherboard. Do not twist either the motherboard or WS9003 during installation.

Optical Cable Installation

Please remove the protectors from the HP transceivers and the cable plugs. Insert the plugs into the connectors of WS9003 until they snap in. The cable configuration is shown below:

Optical Cable Configuration: Full Duplex Mode



If you use the WS9003 in a PC system in junction with WS31xx, please ensure that the piggy back does not collide with components on the PC mainboard such as CPU fans, connectors and power regulators.
Due to the fact that the HP transceiver chipset is getting very hot during operation, we suggest to install a fan in order to lower the temperature of the components.

6.2 Software Configuration

WS9003 occupies only one address location in the address space of the DSP(s): The base address of the SHARC IO-Pack space which is in use. Please refer to your WS3112 or WS2126 manual for the contents of the address map.

1) After power on you have to put WS9003 into the „run“ state by writing a „1“ to bit 2 of the Control Register

2) If WS9003 has to operate with a lower optical bandwidth, it is necessary to set bit 3 in the Trigger Register to "1".

3) The next step is to decide, which SHARC links are used to transfer the data. Let`s assume that DSP link 2 is the transmitter and DSP link 3 is the receiver. We have to set bit 0 to „1“ in the Control Register.

4) Now we have to check (poll) if the optical link is ready for the data transfer. We do this by polling bit 3 of the Control Register until we can read back a „1“.

5) The last thing to do is to enable the DSP interrupt for IRQ1.

Now the link is ready to transmit/receive user data over the specified SHARC links.

7. DSP Interface

WS9003 uses the DSP bus for setup and two out of four DSP links for data transfer.

7.1 Control Register

The Control Register is 4 bit wide and connected to the SHARC bus. Please look at the manual of the motherboard in order to specify the correct base address for the SHARC IO-Pack slot which is in use.

Offset address relative to SHARC IO-Pack slot: 0

Bit #	Read Function	Write Function
3	„1“: TX is ready to transmit data „0“: TX is **NOT** ready to transmit data	-
2	„0“: Chipset is in „RESET“ state „1“: Chipset is in „RUN“ state	„0“: Reset chipset „1“: Put chipset into „RUN“ state
1	„0“: DSP link 3 is selected for RX „1“: DSP link 4 is selected for RX	„0“: Select DSP link 3 for RX „1“: Select DSP link 4 for RX
0	„0“: DSP link 1 is selected for TX „1“: DSP link 2 is selected for TX	„0“: Select DSP link 1 for TX „1“: Select DSP link 2 for TX

Bit 3: This bit represents the status of the optical link. If bit 3 is „1“ then the RX- and TX parts are synchronized and ready to transport data. As long as the link is not ready, the WS9003 logic submitts IRQs to the SHARC DSP (IRQ1). Therefore it is a good idea to enable the DSP IRQ1 only after the status „Link Ready“ is detected for the first time. Otherwise your DSP software will detect IRQs as long as the link is not ready.

Bit2: This status/control bit forces the module into the reset state when cleared to „0“. In this case all communication on the optical link will stop. After writing a „1“ to this location, the link tries to synchronize itself and will set bit 3 if the link is ready.

Bit 1: Selects which link will receive the data from the WS9003. If bit 1 is cleared („0“), link 3 will receive data from WS9003. If bit 1 is set to „1“, link 4 will be the receiving link.

Bit 0: Selects which link will transmit the data to the WS9003. If bit 0 is cleared („0“), link 1 will transmit data to WS9003. If bit 0 is set to „1“, link 2 will be the transmitting link.

7.2 Trigger Register

The Trigger Register is 4 bit wide and connected to the SHARC bus. Please look at the manual of the motherboard in order to specify the correct base address for the SHARC IO-Pack slot which is in use.

Offset address relative to SHARC IO-Pack slot: 2

Bit #	Read / Write Function
3	„0“: Speed up to 40 Mbyte/s „1“: Speed up to 20 Mbyte/s
2	„0“: Trigger line disabled / tristated „1“: Trigger line enabled
1	„0“: Trigger output NOT inverted „1“: Trigger output inverted
0	„0“: Trigger A is routed to DSP IRQ2 „1“: Trigger B is routed to DSP IRQ2

Two trigger lines are bussed between the two SHARC IO-Pack slots. In case that one IO-Pack is able to source one or both of this lines, you can configure the routing and polarity of the trigger line to the DSP(s).

Bit 3: This bit controls the transfer rate on the optical link. If the bit 3 is set to "0" (default) the peak link speed is 40 Mbyte/s. Otherwise the transfer rate is 20 Mbyte/s (peak).
The transfer rate is also dependent of the oscillator which is mounted on WS9003. With a 60 MHz oscillator the optical transfer rate is 180 Mbit/s, with a 80 MHz oscillator, the optical transfer rate is 240 Mbit/s.

Bit2: If this bit is "0" (default) the trigger line is tristated and not routed to the DSP´s IRQ2 pin. In case that bit 2 is set to "1", the trigger line is connected to the IRQ2 of the DSP.

Bit 1: Selects if the trigger line outputshould be inverted or not.

Bit 0: Selects the trigger line - A or B - to be routed to the DSP IRQ2.

7.3 DSP Interrupts

7.3.1 IRQ Caused By Error Conditions

The logic on WS9003 contains internal FIFOs for RX- and TX direction. If any FIFO gets full, the IRQ1 of the DSP is triggered to inform the user that the data may be corrupt.
A second condition for triggering IRQ1 is if the optical link has lost synchronization. Due to the fact that the link resynchronizes itself in most of the cases, it is possible that bit 3 in the Control Register is set to "1" although an
If an IRQ1 occurs, it is necessary to reinitialize WS9003.

7.3.2 Trigger Line IRQ

DSP IRQ2 is used for either trigger line A or trigger line B. The trigger line and it´s polarity is defined in the Trigger Register.

8. SHARC IO-Packs

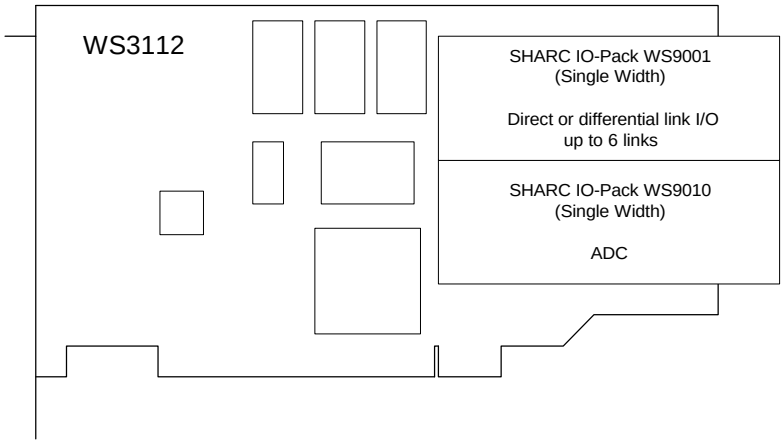
8.1 General Concept

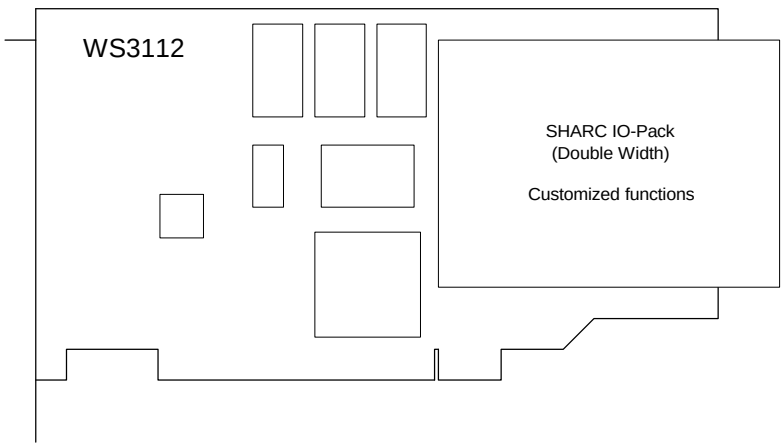
In general the link ports of the DSPs support fast communication between the DSPs and external data sources/sinks up to 40 Mbyte/s for each link *). To keep all options of communication paths, all 6 links of all 6 DSPs are routed to the SHARC IO-Pack front end connector.
A link bus with three links is routed to each DSP by bus jumpers. This allows DSP intercommunication without offboard hardware connections.
A very flexible I/O concept has been realized by introducing the SHARC IO-Packs. Each SHARC DSP now may "carry" a dedicated I/O interface. The range of I/O options may vary from simple link interconnections up to ADCs/DACs I/Os and fiber optic link interfaces.
In customized applications a SHARC IO-Pack also can cover more than one slot.
Depending on the kind of SHARC IO-Pack the SHARC signals which are routed to the front connectors may vary. Please refer to the specification of the SHARC IO-Pack which is in use.

*) The maximum speed is documented in the latest ADSP-2106x data sheet from Analog Devices.

8.1.1 SHARC IO-Packs On WS3112

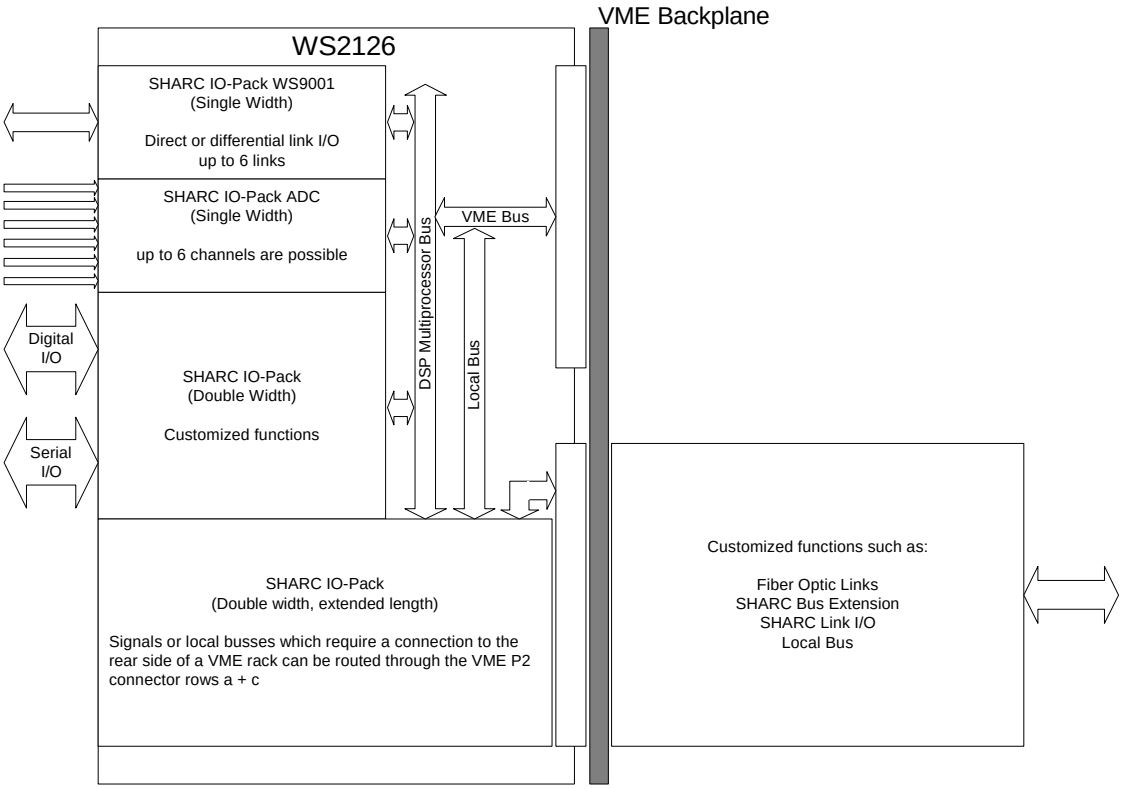
The pictures below pick up a few I/O options to give you an idea how to use SHARC IO-Packs on the PCI master/slave WS3112.





8.1.2 SHARC IO-Packs On WS2126

The picture below picks up a few I/O options to give you an idea how to use SHARC IO-Packs on the VME master/slave WS2126.
Due to the fact that the DSP bus connectors, the local bus connector and the P2 extension connector can be used by a SHARC IO-Pack configuration, the number of I/O alternatives is numerous.



8.2 SHARC IO-Pack Motherboard Connectors

Pin-Nr.	Signal	Description (Front)
1	FLAG3	SHARC Flag 3 Pin
2	TRGC	Trigger Bus C for SHARC I/O-Pack
3	FLAG2	SHARC Flag 2 Pin
4	DGND	Reserved for future use
5	TIMEXP	Timer expired
6	/IRQ1	Interrupt Request Line 1
7	/IRQ2	Interrupt Request Line 2
8	DT1	Data Transmit (SPORT 1)
9	/RST	Board Hardware Reset
10	TCLK1	Transmit Clock (SPORT 1)
11	TFS1	Transmit Frame Sync (SPORT 1)
12	DR1	Data Receive (SPORT 1)
13	RCLK1	Receive Clock (SPORT 1)
14	RFS1	Receive Frame Sync (SPORT 1)
15	DGND	
16	L5ACK	Link Port 5 Acknowledge
17	L5CLK	Link Port 5 Clock
18	L5D0	Link Port 5 Data D0
19	L5D1	Link Port 5 Data D1
20	L5D2	Link Port 5 Data D2
21	L5D3	Link Port 5 Data D3
22	+5VD	
23	DGND	
24	+5VD	
25	L4ACK	Link Port 4 Acknowledge
26	L4CLK	Link Port 4 Clock
27	L4D0	Link Port 4 Data D0
28	L4D1	Link Port 4 Data D1
29	L4D2	Link Port 4 Data D2
30	L4D3	Link Port 4 Data D3
31	DGND	
32	L3ACK	Link Port 3 Acknowledge
33	L3CLK	Link Port 3 Clock
34	L3D0	Link Port 3 Data D0
35	L3D1	Link Port 3 Data D1
36	L3D2	Link Port 3 Data D2
37	L3D3	Link Port 3 Data D3
38	+5VD	
39	I2CSD	I^2C serial data
40	L2ACK	Link Port 2 Acknowledge
41	L2CLK	Link Port 2 Clock
42	L2D0	Link Port 2 Data D0
43	L2D1	Link Port 2 Data D1
44	L2D2	Link Port 2 Data D2
45	L2D3	Link Port 2 Data D3
46	+5VD	
47	DGND	
48	DGND	
49	L1ACK	Link Port 1 Acknowledge
50	L1CLK	Link Port 1 Clock
51	L1D0	Link Port 1 Data D0
52	L1D1	Link Port 1 Data D1
53	L1D2	Link Port 1 Data D2
54	L1D3	Link Port 1 Data D3
55	+5VD	
56	L0ACK	Link Port 0 Acknowledge
57	L0CLK	Link Port 0 Clock
58	L0D0	Link Port 0 Data D0
59	L0D1	Link Port 0 Data D1
60	L0D2	Link Port 0 Data D2
61	L0D3	Link Port 0 Data D3
62	DGND	
63	TRGB	Trigger Bus B for SHARC I/O-Pack
64	TRGA	Trigger Bus A for SHARC I/O-Pack

Pin-Nr.	Signal	Description (Rear)
1	SA0	SHARC address bus (HOST: A2)
2	SA3	SHARC address bus (HOST: A5)
3	SA1	SHARC address bus (HOST: A3)
4	SA4	SHARC address bus (HOST: A6)
5	SA2	SHARC address bus (HOST: A4)
6	SA5	SHARC address bus (HOST: A7)
7	-12V	
8	+5VD	
9	DGND	
10	DGND	
11	/DMAR1	DMA Request 1 (Channel 7)
12	/DMAR2	DMA Request 2 (Channel 8)
13	DGND	
14	ACK	Memory Acknowledge
15	SD17	SHARC data bus (VME: D1)
16	SD32	SHARC data bus (VME: D16)
17	SD16	SHARC data bus (VME: D0)
18	DGND	
19	+12V	
20	SA6	SHARC address bus (HOST: A8)
21	DT0	Data Transmit (SPORT 0)
22	/PIGGY_CS	SHARC I/O-Pack Chipselect
23	TFS0	Transmit Frame Sync (SPORT 0)
24	TCLK0	Transmit Clock (SPORT 0)
25	RCLK0	Receive Clock (SPORT 0)
26	DR0	Data Receive (SPORT 0)
27	SA7	SHARC address bus (HOST: A9)
28	RFS0	Receive Frame Sync (SPORT 0)
29	+5VD	
30	SD18	SHARC data bus (VME: D2)
31	/RD	Memory Read Strobe
32	I2CSLC	I^2C serial clock
33	SD39	SHARC data bus (VME: D23)
34	/WR	Memory Write Strobe
35	SD37	SHARC data bus (VME: D21)
36	SD38	SHARC data bus (VME: D22)
37	SD35	SHARC data bus (VME: D19)
38	SD36	SHARC data bus (VME: D20)
39	SD34	SHARC data bus (VME: D18)
40	SCLK	System Clock (40 MHz)
41	SD33	SHARC data bus (VME: D17)
42	/DMAG2	DMA Grant 2 (Channel 8)
43	SD20	SHARC data bus (VME: D4)
44	/DMAG1	DMA Grant 1 (Channel 7)
45	SD30	SHARC data bus (VME: D14)
46	SD31	SHARC data bus (VME: D15)
47	SD28	SHARC data bus (VME: D12)
48	SD29	SHARC data bus (VME: D13)
49	SD26	SHARC data bus (VME: D10)
50	SD27	SHARC data bus (VME: D11)
51	SD24	SHARC data bus (VME: D8)
52	SD25	SHARC data bus (VME: D9)
53	SD47	SHARC data bus (VME: D31)
54	SD23	SHARC data bus (VME: D7)
55	SD22	SHARC data bus (VME: D6)
56	SD46	SHARC data bus (VME: D30)
57	SD21	SHARC data bus (VME: D5)
58	SD45	SHARC data bus (VME: D29)
59	SD19	SHARC data bus (VME: D3)
60	SD44	SHARC data bus (VME: D28)
61	SD42	SHARC data bus (VME: D26)
62	SD43	SHARC data bus (VME: D27)
63	SD41	SHARC data bus (VME: D25)
64	SD40	SHARC data bus (VME: D24)

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