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SLS

Multibunch Feedback Fast ADC and Fast DAC Setup USER MANUAL

V:1.0



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I. Overview

A. The bunch feedback system parts

- The position detection part receives the beam signals through pickups and normalizes them.
- An ADC is clocked with the machine RF (round 500MHz) and samples the oscillation of each bunch separately.
- The digital processing part buffers and calculates the correction signal based on the ADC sample.
- A DAC is as well clocked with the machine RF (round 500MHz) and converts the calculated correction signals back to an analogue value
- The amplifier scales the correction signals and provides the power to the kicker to generate the fields in order to correct (damp) the bunch oscillation.



Fig. 1 Multibunch feedback system overview.

One of the main problems is a correct setup of the system in order to calculate the correction signal on basis of the previous samples of the same bunch and to kick this particular bunch only.





II. Hardware checks

One of the most important issues to check on the Multi Bunch Feedback system is the clock. The clock is derived from the machine RF (round 500MHz) and used in the FPGA to keep track of a particular bunch. Hence loosing the clock means loosing the information of the bunch number being measured and kicked. This means if the clock is lost then the ADC card is measuring a particular bunch but the DAC is not kicking this bunch but a different one.

Therefore check the LEDs on the VME card frontpanel according to following table.

Please note: The clock lock is as well a part of the alarm handler.

A. ADC LEDs

The ADC VME board has 3 LEDs which visualise the status of the board. The 3 LEDs are denoted as X, Y and Z.

LED	Color	Description	
Х	Off	Should never happen. Check power or hardware	
		defect.	
	Green	The clock system in the FPGA is working properly.	
		Due to the implementation of the clock system this	
		indicates that the RF clock jitter is less than 150ps and	
		no RF clock period was missed.	
	Red	The clock system in the FPGA is NOT working	
		properly. Due to the implementation of the clock	
		system this indicates that the RF clock jitter was/is	
		bigger than 150ps and/or RF clock period was missed.	
	Yellow	Not implemented.	
Y	Off	Currently no VME access to this card.	
	green	VME signalling access.	
	Red	VME signalling acknowledge.	
	yellow	Both of the above.	
Ζ	Z Off VME Commute directing ADC data to ZBT RAM		
		and FPDP interface.	
	green	VME Commute directing ADC data to FPDP interface	
		only.	
	Red	VME Commute directing ZBT RAM buffer data to	
		FPDP interface (a debugging feature).	
	yellow	VME Commute directing ADC data to ZBT RAM buffer	
		only.	







B. DAC LEDs

The DAC VME board has 3 LEDs which visualise the status of the board. The 3 LEDs are denoted as X, Y and Z.

LED	Color	Description	
Х	off	Should never happen. Check power or hardware	
		defect.	
	green	The clock system in the FPGA is working properly.	
		Due to the implementation of the clock system this	
		indicates that the RF clock jitter is less than 150ps and	
		no RF clock period was missed.	
	red	The clock system in the FPGA is NOT working	
		properly. Due to the implementation of the clock	
		system this indicates that the RF clock jitter was/is	
		bigger than 150ps and/or RF clock period was missed	
	yellow	Not implemented.	
Y	off	Currently no VME access to this card.	
	green	VME signalling access.	
	red	VME signalling acknowledge.	
	yellow	Both of the above.	
Ζ	Z off VME Commute directing FPDP data to ZBT R		
		buffer and DAC.	
	green	VME Commute directing FPDP data to DAC only.	
	red	VME Commute directing ZBT RAM buffer data to DAC	
		(a debugging feature).	
	yellow	VME Commute directing FPDP data to ZBT RAM	
		buffer only.	







III. Restore last stable settings

1.) Open one of the Multibunch-Feedback medm applications.

A_DI_MBF_TMBF_Expert.adl					
horizontal	Multi Bunch F	Feedback			
Command: initia	lisation = Cmd Request done	casr all planes: ‼			
ADC-DAC delay [buckets]: 314 Error:OK Code: 0					
ADC clk shift: 1865 ps DAC clk shift: 300 ps	busy 1865 ps (readback) 265 ps (readback)	RFFE: Expert Power Amp.: Expert			
Power Splitter:	Power Splitter: OFF ON				
FIR	Gain	ZBT			
filter coefficients cf0: 14113 cf1: -10425 cf2: 1408 cf3: 1699 cf4: -7891 cf5: 12623 cf6: -15020 cf7: 14637	GB: 3 FIR setting Gain GPB: 9 GB: 490	sampling settings			

Fig. 2 Horizontal MBFB medm application

2.) Press the exclamation mark next to "casr all planes".

) fileSelector		_ 🗆 ×	
		stable		
	directory /home/slsop/common/snapshots			
f	ile	keywords comments		
A	_DI_MBF_init_prod			
F	īle Pattern Keywords Pattern	A_DI_MBF_init_prod_Snapshot Selected File all Show Info History Restore	p Close	
	omments Pattern Me	ssages:		

Fig. 3 Channel Access Save Restore application





3.) Select the needed file (probably the newest one).

4.) Press Restore.

Caution: You are restoring all three planes. The saveres file contains not only the EPICS channels of this particular plane but of horizontal, vertical and longitudinal plane.

Caution: The "ADC-DAC delay [bucket]" and the clock shifter channels for ADC, DAC and MOD are not saved and restored.

The button "Info" of the Channel-Access-Save-Restore shows the difference between the stored and current set EPICs channels.





IV. Calculate the FIR values

A. Setup Longitundinal Multibunch Feedback

5.) Open a terminal and change the directory:

cd /exchange/home/dehler/public/MBF/PUL

6.) Check the content of the 00Settings file:

tail 00Settings

7.) Open octave and copy the desired filter:

octave.bin:1>mbf_setfilter(mbf_alltap(1.8e-3, 3.5e-3, 120,0))

This octave script will set the FIR coefficients for the longitudinal MBFB.

A_DI_MBF_LMBF_Expert.ad1 Iongitudinal Multi Bunch Feedback			
Command:initi	alisation - Cmd Request		
ADC-DAC delay [buck	Kets]: 8477 Error: OK Code: 0		
ADC clk shift: 1400 p DAC clk shift: 1500 p MOD clk shift: 790 p	ps busy 1330 ps (readback) RFFE: Expert ps 1500 ps (readback) Power Amp.: Expert ps 790 ps (readback) Power Amp.: Expert		
FPGA FIR filter coefficie cf0: -24679 cf1: -29622 cf2: -32384 cf3: -32767 cf4: -30770 cf5: -26584 cf6: -20581 cf7: -13272 cf8: -5261 cf9: 2807 cf10: 10305 cf11: 16678 cf12: 21486 cf13: 24443 cf14: 25429 cf15: 24498	IIR Gain ants gain coefficients Gain: 15 FIR Gain gain coefficients Gain: P PGain: P PBunch: #90		

Fig. 4 Longitudinal MBFB





8.) Set "Command" to initialisation and press the "Cmd request" button.

The lonigudinal crate is now set up and running.

There are additional tests in order to see wether the VME cards have synchronized properly.

Open a rmc terminal for ARIDI-VME-MBFS and type the commands adc_status(1) and dac_status(2):

The important information here is that the "**125 MHz clock lock**" is "**1**". This means that the clock was correctly received since the initialisation of the card. The meaning if "**DVALID**" is "**1**" is that the FPGA retrieves bunch information from the ADC, the calculation pipeline was started and the correction data was send to the DAC.

```
ARIDI-VME-MBFS > dac_status(2)
*****
* * *
           D A C PU_DAC
DAC status...
 DAC firmware revision: dac0100
 DAC status: 2210003
 DAC status bits:
  Clock lock: 1
  DAC start
              1
              1
  DVALID
  FIFO empty 0 FIFO Half full
FIFO full 0 FIFO overflow
cq enable 1
                                1
                                 0
 Acq enable
 Commute
              0
          0
 Run mode
```

The important information here is that the "Clock lock" is "1". This means that the clock was correctly received since the initialisation of the card. The meaning of "DVALID" is "1" means that the FPGA receives the correction data from the ADC. If "DAC start" is "1" then the start pulse was received from the ADC. If "FIFO Half full" is "1" then this means that the FPGA buffer contains valid correction data and operates in a valid range (e.g. did not overflow or underflow).





B. Setup Horizontal Multibunch Feedback

1.) Open a terminal and change the directory:

cd /exchange/home/dehler/public/MBF/PUH

2.) Check the content of the 00Settings file:

tail 00Settings

3.) Open octave and copy the desired filter:

octave.bin:1>mbf_alltap(.431,340)

This octave script will set the FIR coefficients for the horizontal MBFB.

A_DI_MBF_TMBF_Expert.adl				
horizontal Multi Bunch Feedback				
Command: initialisation - <u>Cand Request</u>				
ADC-DAC delay Ebuckets Error: <mark>0K</mark>	ADC-DAC delay [buckets]: 314 Error:OK Code: 0			
ADC clk shift: 1865 ps DAC clk shift: 300 ps	1865 ps (readback) 265 ps (readback)	RFFE: Expert Power Amp.: Expert		
Power Splitter:	Power Splitter: OFF ON			
FIR	Gain	ZBT		
filter coefficients cf0: 44113 cf1: 10425 cf2: 4808 cf3: 4699 cf4: -7891 cf5: 12623 cf6: -15020 cf7: 14637	IIR setting IIR disabled IIR enabled GB: 3 FIR setting Gain 6 GPB: 0 GB: 490	sampling settings		

Fig. 5 Horizontal MBFB

4.) Set "Command" to initialisation and press the "Cmd request" button.

The horizontal crate is now set up and running.

There are additional tests in order to see wether the VME cards have synchronized properly.





Open a rmc terminal for ARIDI-VME-MBFX and type the commands adc_status(0) and dac_status(1):

The important information here is that the "**125 MHz clock lock**" is "**1**". This means that the clock was correctly received since the initialisation of the card. The meaning if "**DVALID**" is "**1**" is that the FPGA retrieves bunch information from the ADC, the calculation pipeline was started and the correction data was send to the DAC.

```
ARIDI-VME-MBFX > dac_status(1)
* * *
          D A C PUH DAC
DAC status...
 DAC firmware revision: dac0100
 DAC status: 2210003
 DAC status bits:
  Clock lock: 1
  DAC start 1
             1
  DVALID
 FIFO empty 0 FIFO Half full
FIFO full 0 FIFO overflow
Acq enable 1
                                1
                               0
 Commute
             0
 Run mode
              0
```

The important information here is that the "Clock lock" is "1". This means that the clock was correctly received since the initialisation of the card. The meaning of "DVALID" is "1" means that the FPGA receives the correction data from the ADC. If "DAC start" is "1" then the start pulse was received from the ADC. If "FIFO Half full" is "1" then this means that the FPGA buffer contains valid correction data and operates in a valid range (e.g. did not overflow or underflow).

C. Setup Vertical Multibunch Feedback

1.) Open a terminal and change the directory:

cd /exchange/home/dehler/public/MBF/PUV

2.) Check the content of the 00Settings file:





tail 00Settings

3.) Open octave and copy the desired filter:

octave.bin:1>mbf_alltap(.27,70)

This octave script will set the FIR coefficients for the vertical MBFB.

🗘 A_DI_MBF_TMBF_Expert.adl			
vertical	Multi Bunch F	eedback	
Command: i	nitialisation 🚽 📶	Request one	
ADC-DAC delay [buckets]: 308 Error:OK Code: 0			
ADC clk shift: 1500 ps DAC clk shift: 1445 ps	 1500 ps (readback) 1420 ps (readback) 	RFFE:ExpertPower Amp.:Expert	
Power Splitter:	OFF ON		
FIR	Gain	ZBT	
filter coefficients cf0: 4447 cf1: -16742 cf2: -250 cf3: 16805 cf4: -3962 cf5: -15812 cf6: 7926 cf7: 13825	IIR setting IIR disabled IIR enabled GB: 3 FIR setting Gain GPB: 0 GB: 490	sampling settings	

Fig. 6 Vertical MBFB

4.) Set "Command" to initialisation and press the "Cmd request" button.

The vertical crate is now set up and running.

There are additional tests in order to see wether the VME cards have synchronized properly.

Open a rmc terminal for ARIDI-VME-MBFY and type the commands adc_status(2) and dac_status(3):





```
ADC firmware revision: adc0207
ADC status: 200003
ADC status register:
125 MHz clock lock: 1
DVALID: 1 Reset flag: 0
```

The important information here is that the "125 MHz clock lock" is "1". This means that the clock was correctly received since the initialisation of the card. The meaning if "DVALID" is "1" is that the FPGA retrieves bunch information from the ADC, the calculation pipeline was started and the correction data was send to the DAC.

```
ARIDI-VME-MBFY > dac_status(3)
* * *
           D A C PUV_DAC
DAC status...
 DAC firmware revision: dac0100
 DAC status: 2210003
 DAC status bits:
  Clock lock: 1
  DAC start
             1
             1
  DVALID
  FIFO empty 0 FIFO Half full
FIFO full 0 FIFO overflow
cq enable 1
                               1
                               0
 Acq enable
 Commute
              0
 Run mode
              0
```

The important information here is that the "Clock lock" is "1". This means that the clock was correctly received since the initialisation of the card. The meaning of "DVALID" is "1" means that the FPGA receives the correction data from the ADC. If "DAC start" is "1" then the start pulse was received from the ADC. If "FIFO Half full" is "1" then this means that the FPGA buffer contains valid correction data and operates in a valid range (e.g. did not overflow or underflow).